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Service Manual

CIRCUIT DESCRIPTIONS

SV-28i

SV-25i
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COLOUR TELEVISION

FOR REPAIR AND ADJUSTMENT: REFER TO PRT-009

CONTENTS

PART I

	Page
1. BLOCK DIAGRAM	3
2. SOPS	4
2.1 Introduction	4
2.2 Working in the TV mode	4
2.3 The 5 Volt power supply for the microprocessor	8
2.4 Automatic degaussing	10
3. THE FRONT-END MODULE	11
3.1 Tuner part	11
3.2 IF-part	11
4. LUMINANCE AND CHROMINANCE CIRCUIT	12
4.1 Luminance filter circuit	12
4.2 Chrominance circuit	12
5. VIDEO CONTROL	13
5.1 Introduction	13
5.2 TDA 4580	13
6. RGB AMPLIFIERS	14
6.1 DC adjustment at black level	14
6.2 Amplification	14
6.3 DC setting	14
6.4 Cut-off point stabilisation	15
6.5 Beam current limiter	15
7. THE SOUND PATH	16
7.1 Block diagram	16
7.2 The demodulators	16
7.3 The stereomatrix	16
7.4 The switching unit	17
7.5 Switching over sound with scart	17
7.6 The identification circuit	17
7.7 TDA 3810	18
7.7.1 Stereo-mono	
7.7.2 Spatial on stereo	
7.7.3 Spatial on mono	
7.8 Driver stage for IC 7145	20
7.9 Controlled amplifier TDA 1524	20
7.10 The output amplifiers	21
8. SYNCHRONIZATION CIRCUIT	22
8.1 Block diagram	22
8.2 Input circuit and video switch	22
8.3 Horizontal sync. separator	22
8.4 Oscillator, detectors Q1 and Q2 and output stage	24
8.4.1 Q1 detector	
8.4.2 Sawtooth generator	
8.4.3 Q2 detector	
8.4.4 Hor. pre-amplification stage	
8.4.5 Sync. composite sync. pulse (S.C.S.)	
8.5 Vertical synchronization	26
8.5.1 Frame integrator and clippers	
8.5.2 PAL anti-copy guard	
8.5.3 Sawtooth generator	
8.5.4 Starting up of sync. IC	

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Page

9. FRAME OUTPUT AMPLIFIER 28

10. HORIZONTAL OUTPUT STAGE 29

10.1 Horizontal deflection circuit 29
10.2 East-West correction 30
10.3 High voltage 30
10.4 Derived supply voltage 30

11. PICTURE TUBE CORRECTIONS 30

12. TXT DECODER, SEE CIRCUIT DESCRIPTION: COMPUTER CONTROLLED TELETEXT

13. THE FST-6 CONTROL SYSTEM 31
13.1 Introduction 31
13.1.1 Block diagram
13.1.2 Control possibilities
13.2 Control 32
13.2.1 Remote control
13.2.2 Local keyboard and display
13.3 Tuning procedure 34
13.4 Analogue controls 34
13.5 Memory drive 36
13.6 Error diagnosis 37

Circuit Diagram A
Circuit Diagram B
Circuit Diagram C

PART II. (Computer Controlled Teletext)

Page

1. INTRODUCTION 3

1.1 Characteristics of CCT 3
1.2 Block diagram TIC TAC TROM decoder 3
1.3 Block diagram CCT decoder 4
1.4 Circuit diagram CCT decoder 4

2. VIDEO INPUT PROCESSOR VIP2 5

2.1 Block diagram 5
2.2 Circuit diagram 5

3. MICROCOMPUTER CIRCUIT 6

3.1 Introduction 6
3.2 CPU and Memory 6
3.3 Oscillator and Clock 6
3.4 IIC Interface 6
3.5 Operation 6
3.6 Language selection 6
3.7 Reset 7
3.7.1 Power On Reset 7
3.7.2 Voltage guard 7
3.7.3 Self-resetting 7

4. CCT-IC 8

4.1 Introduction 8
4.2 Block diagram 8
4.3 IIC Interface and CCT control 8
4.3.1 Format of IIC transfers 8
4.3.2 CCT control registers 8
4.4 Data Acquisition function 10
4.4.1 Data Acquisition Principles 10
4.4.2 Page request 10
4.4.3 Ghost Rows 12
4.4.4 Multipage decoder 13
4.4.5 Full-Channel Mode 13
4.4.6 Block diagram 13
4.4.7 Stored data 14

Page

4.5 Timing Chain function 17
4.6 Character Generator function 18
4.6.1 Introduction 18
4.6.2 Formation of alphanumerical characters 18
4.6.3 Formation of graphic characters 18
4.6.4 Control characters 20
4.6.5 Possibilities of language selection 20
4.6.6 Page attributes 22
4.6.7 Adressing the ROM 22
4.6.8 Data output 22
4.6.9 Text format and Timing 23
4.6.10 Display Control 23
4.7 Memory Interface Function 24
4.7.1 Block diagram 24
4.7.2 Memory configuration 25

5. PAGE MEMORY 26

5.1 Circuit diagram 26
5.2 Memory control 26
5.3 Reading data 26
5.4 Writing data 26

6. INPUT AND OUTPUT CIRCUITS 27

6.1 MIBUS circuit 27
6.2 RGB circuit 27
6.3 Auto Interlace circuit 28
6.4 Blanking circuit 28

APPENDICES 29

A. IIC bus 29
B. CCT Register Functions 31
C. Circuit diagram CCT decoder 37
D. List of Terms and Abbreviations 39

Service Manual

REPAIR & ADJUSTMENTS

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THIS SERVICE MANUAL IS APPLICABLE TO SV-28i, SV-25i AND SV-21i MODELS WHICH ARE DISTINGUISHED AS BO,BE,BN,BNN,IF, SO AND ME.

FOR REPAIR AND ADJUSTMENT REFER TO SERVICE MANUAL PRT-009 WITH THE EXCEPTION OF THE FOLLOWING PARTS:

DESCRIPTION	PARTSNUMBER
SPEAKER GRILLE	4822 701 10985
FRONT HOUSING	4822 701 10986
DOOR FLAP	4822 701 10987
MASK 21"	4822 701 10978
MASK 25"	4822 701 10979
MASK 28"	4822 701 10981
CABINET 21"	4822 701 10537
CABINET 25"	4822 701 10581
CABINET 28"	4822 701 10579
FOOT	4822 701 10988
REAR COVER 21"	4822 701 10982
REAR COVER 25"	4822 701 10983
REAR COVER 28"	4822 701 10984
REMOTE CONTROL	3104 308 71400
INSTRUCTION LABEL	3104 305 84020
LEARN LABEL	3104 305 84011
OPERATING INSTRUCTIONS	3104 305 25701
BOX 21"	4822 701 10975
BOX 25"	4822 701 10976
BOX 28"	4822 701 10977

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BLOCKDIAGRAM

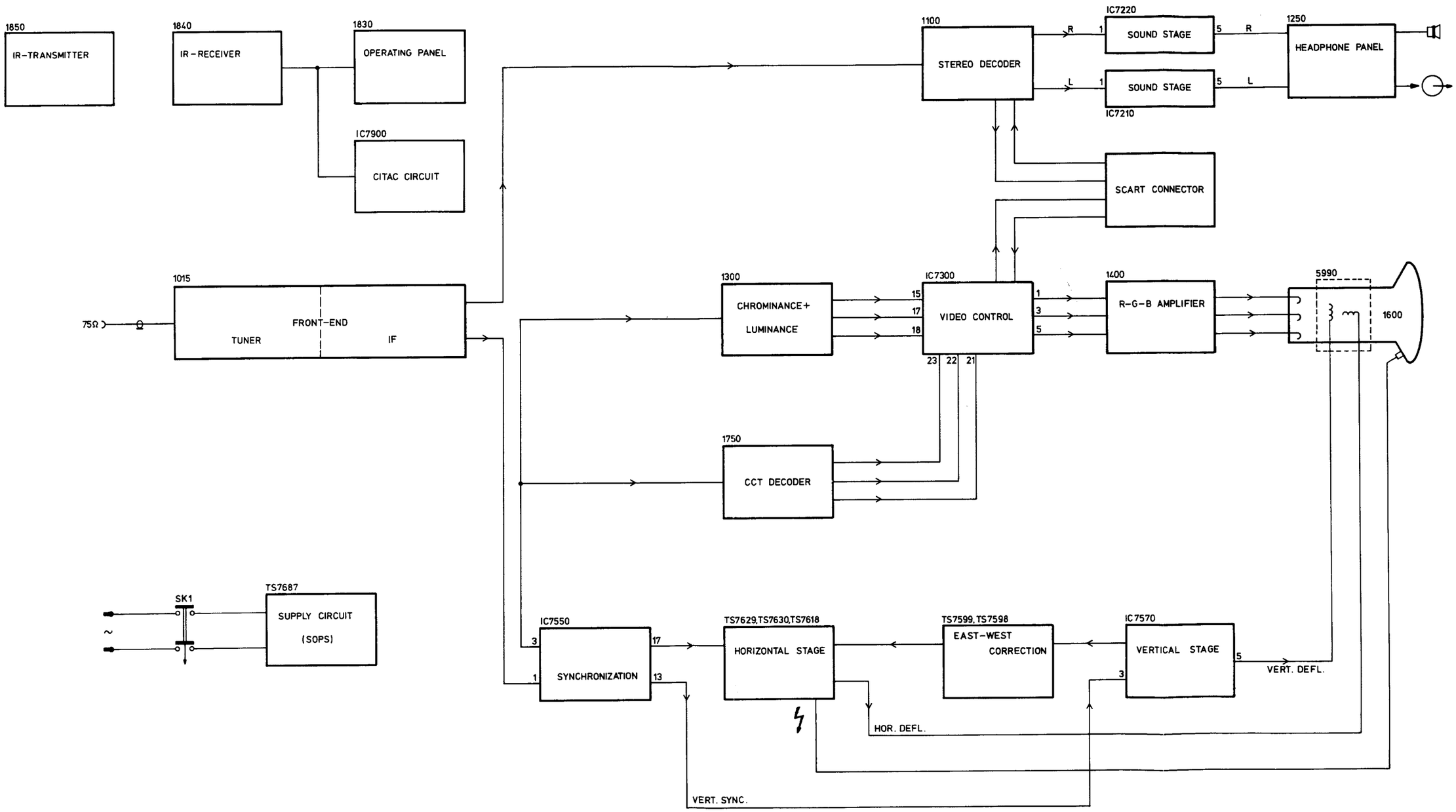

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Fig. 1-1

1. BLOCK DIAGRAM (Fig. 1.1)

In the 2B system, most of the sub–circuits are integrated on the chassis.
Only the R.G.B. amplifiers (on the picture tube PCB) and the optional circuits such as the front–end (Tuner + IF), control, stereo decoder, headphones, chrominance + luminance and the CCTdecoder are accomodated on separate PCB's.
The chassis consists of the following blocks (Fig. 1–1).

1. At position 1015 is a front–end which consists of a channel selector part and a IF–part which consists of the IF–amplifier, IF–detectors the AFC and the AGC circuits.
2. At position 1100 is a stereo–decoder which drives two sound output stages (2 x 10W)
3. At position 1300 is the chrominance and luminance circuit, the video control circuit consists of separate components which are mounted on the chassis, this circuit drives the R–G–B amplifiers.
4. The R–G–B amplifiers are situated on the picture tube PCB at position 1400. There are three possible versions of picture tubes.
   1. 21 inch 90° FSQ
   2. 24 inch 110° FSQ
   3. 28 inch 110° FSQ
5. At position 1750 is the CCT–decoder for the decoding of the teletext signals.
6. For the control system has been applied the CITAC–IC7900, the control system has been integrated on the chassis. The keyboard and microprocessor have been applied at position 1830. CITAC stands for Computer Interface for Tuning and Analogue Control and this IC supplies the band switching voltages and the control voltage for volume, etc.
7. The centre of the sync. circuit is TDA 8370 at position 7550.
8. The horizontal output stage, the east–west correction and the vertical output stage have all been accomodated on the chassis.
   As the required east–west corrections for the 21 inch, 24 inch and 28 inch picture tube are different, some components have been changed.
   The line output transistor at position 7618 is 2SD157PH. In the vertical output stage the TDA 3653 AQ for 90° has been applied at position 7570 and the TDA 3654Q has been applied at position 7570 for 110°
   The line output stage also supplies several supply voltages.
9. The mains isolated power supply is a SOPS. SOPS stands for Self Oscillating Power Supply, Here the supply is not synchronised by line pulses from the sync. circuit.
   The drive for the line output stage does take place, of course, from the sync circuit via an amplification stage.

2. MAINS ISOLATED POWER SUPPLY (SOPS)

2.1 Introduction

The abbreviation S.O.P.S. stands for self-osc power supply.
The S.O.P.S. is equipped as a mains-isolatec supply and is suited for mains voltages from 2.. .240 V (± 10%).
The output voltage is 140 V for supply of the line output stage; 18 V for the sound output stage and 5 V for the supply of the microprocessor in the control system.
The central part of the power supply is formed by a blocking oscillator, with a frequency varying from 20 kHz to
60 kHz and nominally about 40 kHz and a pulse-width modulator checking the blocking oscillator.
The pulse-width modulator in its turn is driven by information concerning the output voltage via an opto-coupler and by information concerning the mains voltage. The power supply is protected against overload, overvoltage and unloaded or short-circuited output.
If the TV set is switched in the Stand-by mode, the S.O.P.S. power supply delivers 5 V to the microprocessor in the control system. Contrary to former sets which required a separate power supply for the Stand-by mode. In the stand-by mode all other circuits are offered a voltage that is far below the nominal value, so these circuits will not operate.

2.2 Working in the TV mode

2.2.1 Principle working (see Fig. 2-1)

In principle the power supply consists of three blocks, viz.: blocking oscillator block A, pulse-width modulator block B and the control circuit, block C, which via opto-coupler 7668 feeds back its information to the pulse-width modulator. The +140 V voltage which is checked and stabilized by the control is the power supply voltage for the line output stage. The control ensures that the pulse-width modulator switches the blocking oscillator on and off at the right moment and this such that there will be equilibrium between the power consumption and the power dissipation. During the time that the blocking oscillator is switched off, energy is delivered to the load. If the blocking oscillator is switched on again, energy is consumed from the mains.
Windings 1-11 and 1-2 deliver voltage to the pulse-width modulator allowing it to determine the switch-off moment for TS7687.

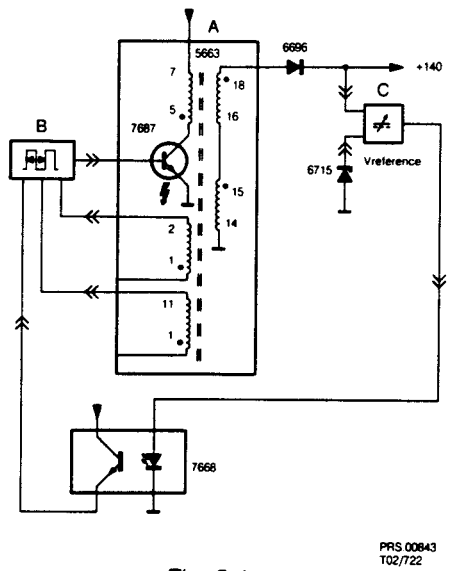

Fig. 2-1

2.2.2 Blocking oscillator and pulse-width modulator

The blocking oscillator which forms the basis of the S.O.P.S. is started via R3686 (see Fig. 2.2).
The starting voltage across C2658 is obtained by means of diodes 6655 and 6654 and R3657 and R3656.
The average voltage that results here is about 125 V.
During normal TV operation TS7687 is driven by the voltage across winding 1-9 which is coupled magnetically to primary winding 5-7.
These windings have the same winding direction. This is indicated by fat dots in the related figures.
The voltage across secondary windings 14-15 and 16-18 of transformer 5663 is rectified by D6696 from which the 140 V for the power supply of the line output stage is obtained.
If TS7687 is conducting, there is a constant voltage of +280 V present across winding 5-7 and as a result a linearly increasing current is flowing through this winding (see Fig. 2-3).
Windings 14-15 and 16-18 do not deliver current because the voltage across these windings has a negative polarity. As a result magnetic energy is stored in transformer 5663 during t_0-t_1.
If transformer 5663 gets saturated by the linearly increasing current, winding 1-9 is no longer kept on voltage and the base current delivered by winding 1-9 drops out at point of time t_1.

Transistor 7687 stops conducting and primary winding 5-7 now possesses a certain quantity of magnetic energy. The voltage across winding 5-7 reverses its polarity and D6664 starts conducting.
When TS7687 is out of conduction, a linearly increasing voltage is built across C2664.

The final value of the voltage across C2664 is approx 550 V. (Vce TS7687 is approx 550 V).
At point of time t_1 the voltage across secondary windings 14-15 and 16-18 reverses polarity. Via D6696 a linearly decreasing current starts to flow to C2697. (See Fig. 2-3).
At point of time t_2 the secondary current becomes zero and the magnetic energy of transformer 5663 has been transferred to i.a. C2697. Now capacitor 2664 forms an oscillation circuit with winding 5-7 so that an oscillation is developed during t2-t3. Via the magnetic coupling the voltage across winding 1-9 will reverse polarity thus delivering a base current to TS7687. This transistor starts conducting and then the described cycle is repeated.
To limit voltage peaks on the collector of TS7687, the circuit C2664, diode D6664 and R3664 has been applied.

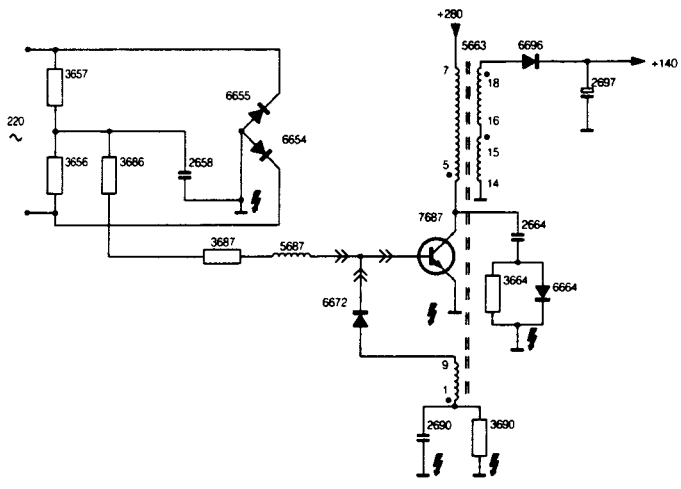

Fig. 2-2

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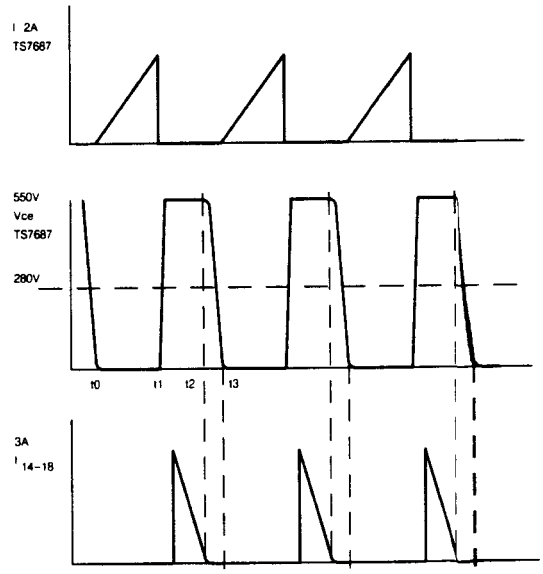

Fig. 2-3

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The pulse-width modulator is fed with three input signals (see Fig. 2-4).
- The voltage from winding 1-11 during the time TS7687 is conducting.
- The voltage from winding 1-2 during the time TS7687 is not conducting.
- The opto-coupler current.

During the time transistor 7687 is conducting winding 1-11, which is coupled magnetically with primary winding 5-7, is offering voltage to the pulse-width modulator. Via D6667, R3678 and R3679 this voltage is integrated by C2675 so that the voltage across this capacitor is increasing. At the lower side of C2675 a negative reference voltage is present, coming from R3690 and C2690.
This reference voltage is variable and is built via two ways during the time TS7687 is conducting.
The first way results because the voltage across winding 1-2, which is coupled magnetically with winding 5-7, is rectified by D6689 (see I1 in Fig. 2-4). The second way results because the voltage across winding 1-9 is rectified by D6672 (see I2 in Fig. 2-4).
The average negative reference voltage is approx -3,5 V. If the threshold voltage of TS7685 is exceeded, TS7685 starts conducting.
Because TS7686 also starts to conduct now, the negative voltage across C2690 of about 3,5 V is passed on to the base of TS7687 as a result of which the base emitter zener voltage of TS7687 is reached. The consequence is that TS7687 is switched off very rapidly.
During the time TS7687 is not conducting transistor 7686 starts to conduct inversely via R3671, D6671, D6670, R3670 and winding 1-9 (see Fig. 2-6).
During switching-off of TS7687 capacitor 2690 is partially discharged.
During the time TS7687 is not conducting the voltage across winding 1-2, that depends on the load by D6675, is rectified (see I3 in Fig. 2-4).
The voltage at point A relative to ground will then be approx -7 V (see Fig. 2-6). Measured at the input of TS7685 this will be approx -5,5 V at nominal load (see Fig. 2-5).
The opto-coupler current is a direct picture of the development of the secondary output voltage. If the load decreases, the opto-coupler current rises so that the voltage across C2675 increases more rapidly as a result of which TS7685 is switched on sooner.
Consequently, via TS7686, TS7687 is switched off sooner (see Fig. 2-5).

2.2.3 Voltage stabilization

A variation in the load at the secondary side of transformer 5663 leads to a voltage variation across C2697 (see Fig. 2-7). This variation in voltage is by control circuit block A compared with a fixed reference voltage across D6715 and converted into a varying current through the diode part of opto-coupler 7668.
This variation is reported optically to the transistor part of the opto-coupler. As a result the pulse-width modulator will switch off sooner or later via TS7687. If the secondary voltage increases, the current through the opto-coupler will increase. Now the pulse-width modulator will take care that TS7687 is switched off sooner.
Because TS7687 is switched off sooner, less energy will be stored in transformer 5663. Consequently, the secondary voltage decreases.
If the secondary voltage decreases, the opto-coupler current will decrease and the pulse-width modulator will switch off TS7687 later.
More energy is stored in the transformer so that the secondary voltage increases again. This causes stabilization of the output voltage.

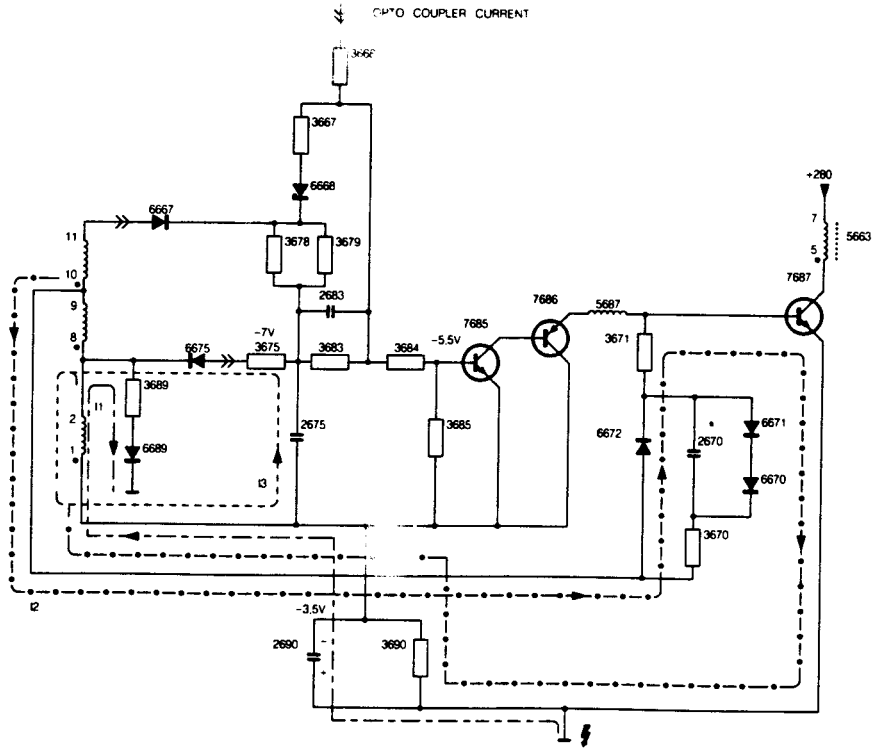

Fig. 2-4

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The load directly affects the frequency at which the power supply is operating (see Fig. 2-5). If the load increases, the primary current will increase. The current through the collector of TS7687 increases by increasing the time this transistor is conducting. The frequency is decreasing now. The maximum conduction time of TS7687 is reached at maximum power dissipation (Po maximum). A minimum frequency is used here.
The minimum conduction time is reached at minimum power (Po minimum).
This is associated with a maximum frequency.
The control circuit (block A in Fig. 2-7) controls output voltage Vo by means of the electronic control with TS7717 and TS7719, see Fig. 2-8.
Via R3719 transistor 7719 takes care of the opto-coupler current through the diode part of opto-coupler 7668.
Secondary winding 14-15 delivers via D6711 across C2712 the power supply voltage for the electronic control. Via R3697, R3705, R3714 and R3715 a test voltage is derived from the +140 V output voltage. From the difference between the reference voltage across D6715 and the derived test voltage TS7717 and TS7719 do now derive a control current for opto-coupler 7668. This control current drives via the transistor part of opto-coupler 7668 the pulse-width modulator (see Fig. 2-7). Ultimately, the pulse-width modulator will determine the switching-off moment of TS7687 thus affecting output voltage Vo.
In the normal control range D6705 is not conducting (see Fig. 2-8).
Secondary winding 19-20 delivers approx +20 V for the sound circuit.
This voltage is not checked by the control circuit so that this voltage will vary with the load by the sound circuit. This winding also delivers its voltage to the sync circuit during start-up of the S.O.P.S. Afterwards the sync circuit is provided with voltage from the line output transformer.

2.2.4 Mains voltage variations

A varying mains voltage results in a varying rectified voltage V_i.
Rectified voltage V_i is approx +280 V (see Fig. 2-7). If rectified voltage V_i rises, the current is with a steeper slope sent through winding 5-7 of transformer 5663. If rectified voltage V_i drops, the slope of the linearly increasing current will decrease. Since the pulse-width modulator receives its information Via winding 1-11 when TS7687 is conducting, a voltage increase or a voltage drop is immediately detected by the pulse-width modulator. If input voltage V_i increases, TS7687 will be switched off sooner by the control so that not too much energy is stored in transformer 5663 and the secondary voltage remains at its stabilized level.
If the voltage decreases, TS7687 is switched off later so that not too little energy is stored in transformer 5663 and the secondary voltage level is stabilized at approx +140 V.
A higher input voltage V_i causes as a result of earlier switching off of TS7687 an increase of the frequency at which the S.O.P.S. is working. A lower input voltage V_i causes as a result of later switching-off of TS7687 a decrease of the frequency.
To ensure that the maximum power dissipation (Po maximum) remains constant at this varying input voltage V_i, the circuit formed by D6668 and R3667 has been applied (see Fig. 2-4).
The frequency fs of the S.O.P.S. varies between 60 kHz and 20 kHz.
At a nominal load and a nominal mains voltage the S.O.P.S. works at a frequency fs of 40 kHz.

2.2.5 Overvoltage protection

This protection serves to prevent damage to the connected circuits and is realized by detection of the line pulse at pin 6 of line output transformer 5620 (see Fig. 2-9). It works as follows:
The normal positiv amplitude of the line pulse at pin 6 is approx 14 Volt. If the line pulse increases to approx 16 Volt, thyristor 6698 is brought in conductance via D6701, D6700 and D6699.

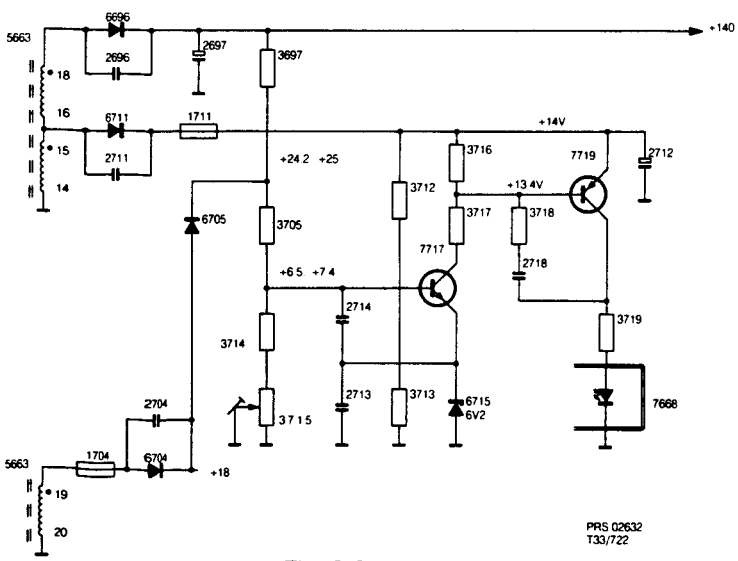

Fig. 2-8

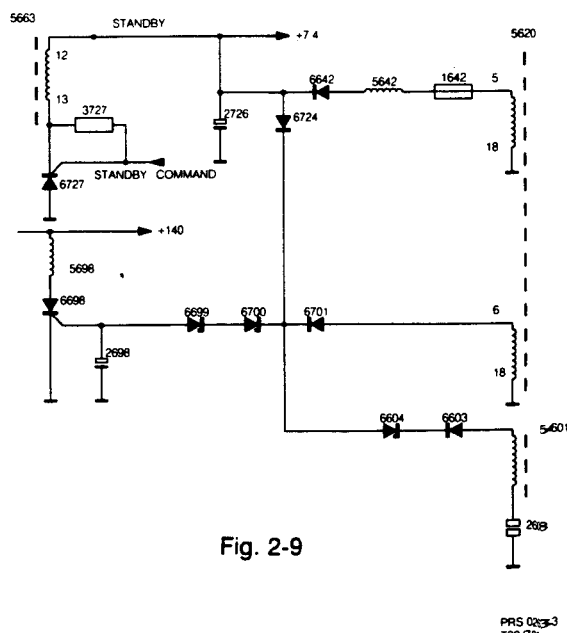

Fig. 2-9

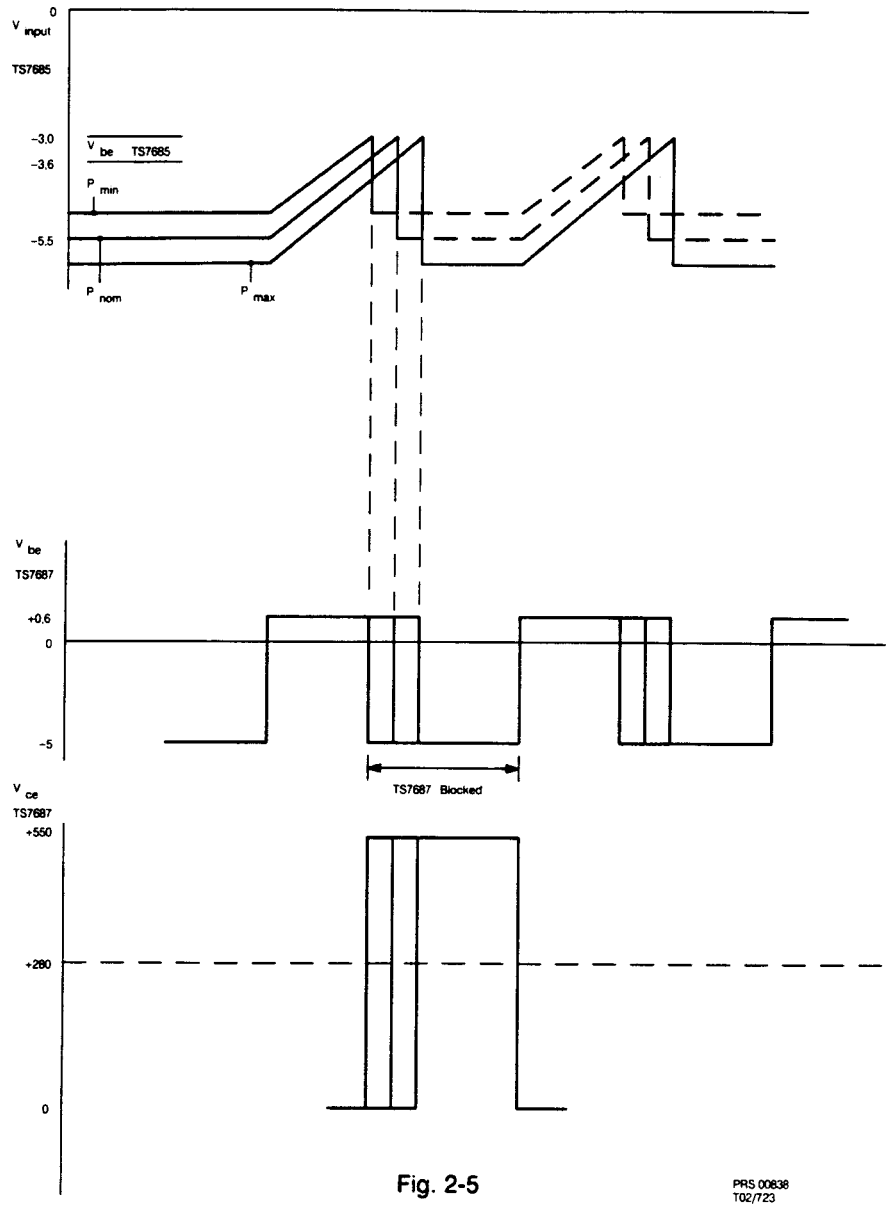

Fig. 2-5

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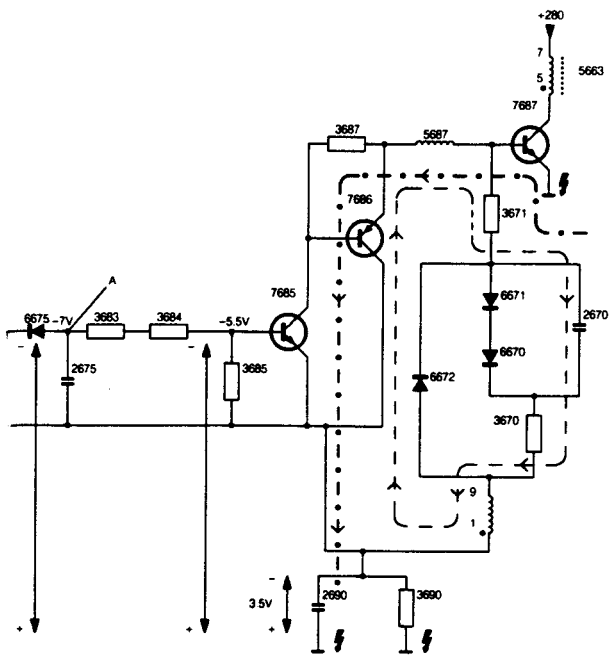

Fig. 2-6

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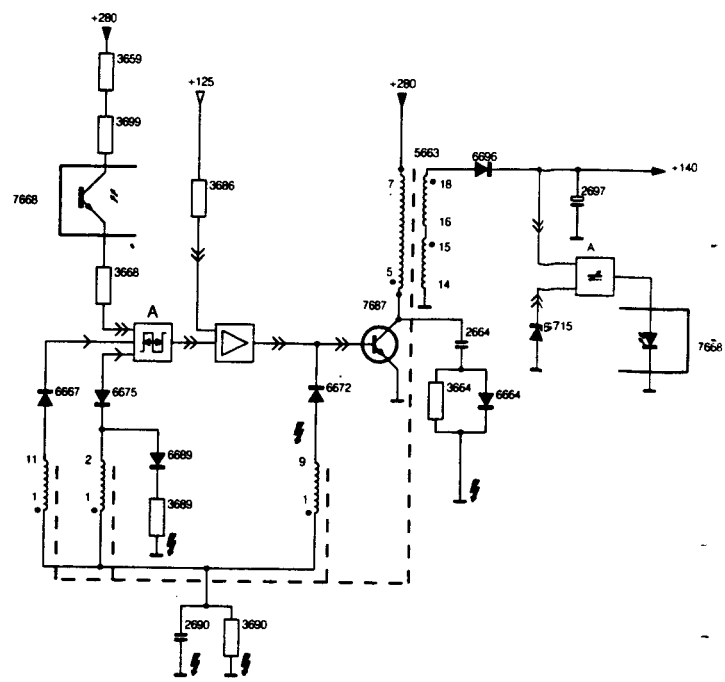

Fig. 2-7

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As a result the output voltage Vo of +140 V is short-circuited. In this way an overvoltage situation is converted into a short-circuit situation (see chapter 2.2.6).
The voltage at pin 5 of line output transformer 5620 is rectified by D6642. This results in a DC voltage of approx 7,4 V across C2726.
This voltage of +7,4 V is not capable of bringing thyristor 6698 into conductance. In the stand-by mode the +7,4 V is delivered by winding 12-13 of transformer 5663. If, however, overvoltage occurs in the stand-by mode the +7,4 V rising to approx 15 V, thyristor 6698 is brought into conductance via D6726. As a result the over-voltage situation is again converted into a short-circuit situation and the voltage is incapable of rising any further.
In case of an interruption in line output transformer 5620 too high a voltage is detected across S5601 in the East-West circuit.
Via D6603 and D6604 the voltage is led to the input circuit of D6698. Via D6700 and D6699 the gate of the thyristor is driven when the peak voltage across S5601 increases to approx 65 V and the result is once again a short-circuit situation thus preventing further damage in the circuit around line output transformer 5620.

2.2.6 Short-circuit protection

In case of a short-circuited output Vo the power supply is operating from a lower frequency of approx 1,3 kHz. The collector peak current of TS7687 has become very small because of the fact that the negative voltage across C2675 has been reduced to a very low value. Transistor 7687 is conducting for only a very limited period of time and very little energy is stored in transformer 5663 during this brief period.
The collector emitter peak voltage of TS7687 has been reduced to maximum approx +325 V.
Through the short-circuit flows secondarily a current of approx 1A (see Fig. 2-10).
This current is delivered as long as the short-circuit continues to exist and the power supply itself remains completely intact (short-circuit resistant).
In case of an overvoltage situation the short-circuit is caused by thyristor 6698 (see 2-9). During the very brief period D6696 is not conducting, thyristor 6698 remains in conductance as a result of its storage time which is greater than the non-conductance time of D6696. By switching off the TV set this short-circuit situation can be eliminated.
(If after switching on a new overvoltage develops, the short-circuit state will return).

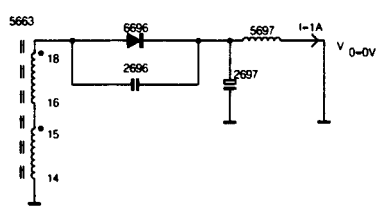

Fig. 2-10

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T33/722

2.2.7 Unloaded state

In the unloaded state the secondary voltage will be inclined to increase since at the primary side of transformer 5663 energy is fed.

Via opto-coupler 7668 TS7687 is switched off for some time until the voltage at the secondary side has dropped sufficiently as a result of the load.
Next the power supply is starting up again for a brief period of time and is immediately switched off then.
This cycle has a repetition time of approx 10 m Sec. The voltages are secondarily slightly above their nominal values. This state is eliminated the moment the circuits are secondarily loaded again.
In case of an interruption in winding 16-18 or an interruption in D6696 a higher voltage will appear across winding 19-20 (see Fig. 2-8). Diode 6705 will start conducting then.
As a result the electronic control will be fed a voltage at its input so that the protection continues to be operative.

2.2.8 Overload

In case of overload, the power supply is in phase III of the characteristic shown in Fig. 2.11.

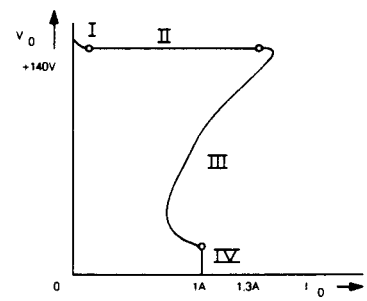


Fig. 2-11

PRS 00816
T02/722

I. Unloaded power supply
II. Normal adjusting range
III. Overload
IV. Short–circuit

The maximum collector current through TS7687 is limited by the pulsewidth modulator.
This current runs through TS7687 at the moment the control current of optocoupler 7668 has become zero. The output voltage Vo of the power supply now is not further stabilized. Consequently, the output voltage Vo will decrease if an overload occurs. This also means a decrease of the negative voltage on C2675. As a result, TS7687 will be be switched off sooner, so that the load current Io eventually decreases again.

2.3 The 5 V power supply for the microprocessor

With the circuit of F[illegible]-12 a stabilized voltage of 5 V is delivered to the m[illegible]cessor. This happens during normal TV operat[illegible]also in the stand-by mode. The latter [illegible]trary to [illegible]ets which required separate power supplies.

2.3.1 Working in normal TV mode

In the TV mode the power supply voltage for the microprocessor is delivered via pin 5 of line output transformer 5620. This voltage is rectified by means of D6642 and smoothed by C2726.
Across C2726 the voltage is approx 7,4 V (See Fig. 2-12). This voltage is fed to CITAC circuit. TS7735 stabilizes the offered voltage of +7,4 V to +5 V. The reference voltage for the stabilization circuit is present across D6741, at the base of TS7735 and across C2735.
The circuit consisting of TS7738, R3739, R3741 and D6739 gives upon switching-on a reset pulse for the microprocessor, thus restarting this microprocessor.
A reset pulse develops via TS7738 upon switching-on because this transistor starts to conduct at a certain moment when the 7,4 V voltage is present across C2726. R3741 and D6739 limit the reset pulse to circ. 1,4 V.

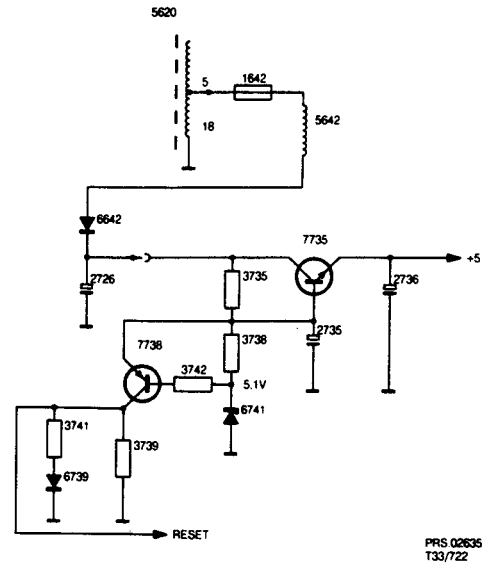


Fig. 2-12

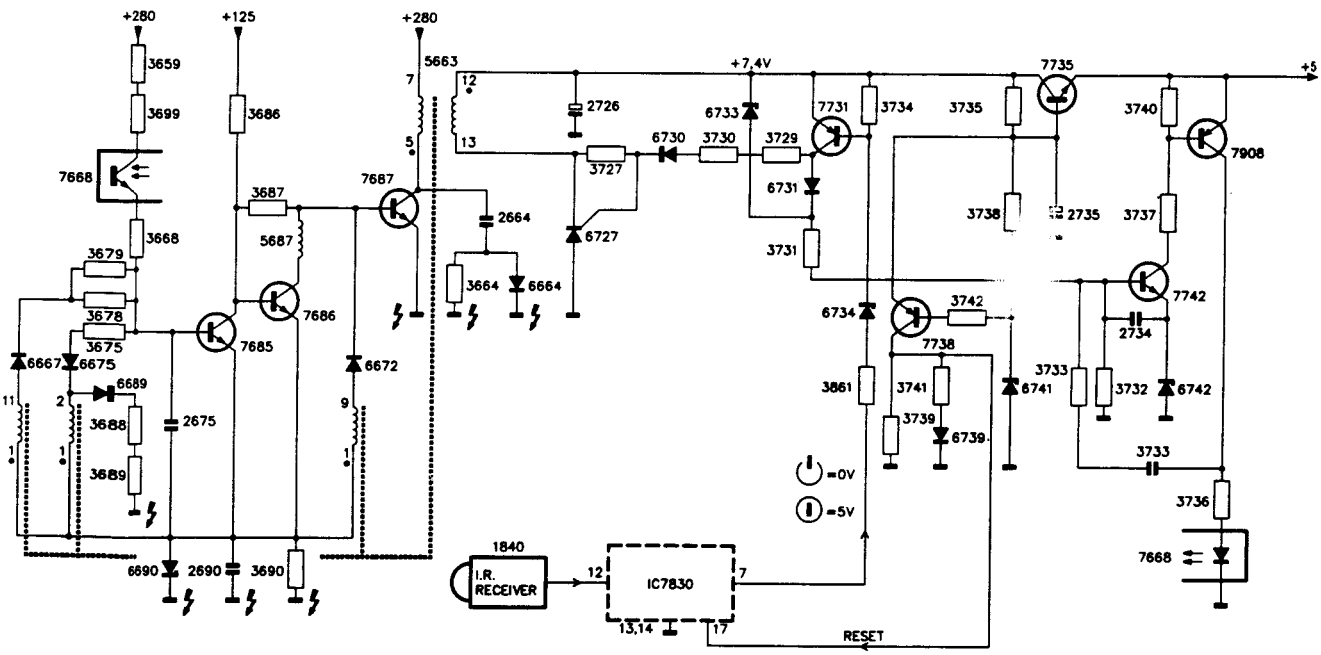


Fig. 2-13

42 232 C12

2.3.2 Working in stand-by mode

Via the receiver of remote control 1840 the stand-by command arrives at pin 12 of microprocessor IC7830 (see Fig. 2-13).
Driven by its program the microprocessor generates a low level at pin 7 (stand-by = 0 V).
If via the keyboard program + or program – is keyed or a program or channel is selected via the transmitter of the remote control, the microprocessor will generate a high level at pin 7 (TV mode = 5 V).
As a result the TV set is switched on again. If a low level is present at pin 7 of the microprocessor, TS7731 starts conducting via R3862 and D6734. As a result thyristor 6727 starts conducting via R3729, R3730 and D6730.
The voltage across winding 12-13 of transformer 5663 is rectified by thyristor 6727 thus forming a DC voltage of approx 7 V across C2726. TS7735 gives a stabilized voltage of 5 V for the power supply of the microprocessor. Via D6731 and R3731, TS7742 is brought in conductance and also TS7908 becomes conductive. Via TS7908 and R3736 opto-coupler 7668 is then driven by the stabilized voltage of 5 V.
Variations in voltage of the 7 V across C2726 affect via D6733, R3731 the current through TS7742, TS7908 and opto-coupler 7668.
An increase in the 7 V voltage results in an increase in the opto-coupler current.
This increase in the current gives at the primary side of transformer 5663 a decrease in the negative voltage across C2690 (see Fig. 2-13).
If the voltage at the base of TS7685 exceeds the base-emitter voltage (Vbe), it will start conducting. Via TS7686 TS7687 will be switched off then at point of time t2 in Fig. 2-14. There will be no primary current Ic through TS7687 and at the secondary side of transformer 5663 the voltage across 12-13 slowly starts to decrease because no new energy is being fed (see Fig. 2-14).
If the voltage across winding 12-13 drops to approx 5,5 V at point of time t1, the opto-coupler current will decrease so much that TS7685 can no longer continue to conduct. The power supply is switched on again via starting resistor 3686. During switching-on the voltage at the base of TS7685 will be approx -2,2 V. Compared with a normally operating S.O.P.S. this is a rather low negative voltage, for the voltage will then be approx -5,5 V.
After a primary current Ic has briefly flown through TS7687, a switching-off pulse is given by winding 1-11. This pulse causes via D6667 and R3678 and R3679 a very short peak voltage across C2675.
This peak voltage drives TS7685 very briefly into conductance but since there is not enough negative voltage across C2690, TS7687 is kept switched off only very briefly. After this short period of non-conductance of TS7687 this transistor is via starting resistor R3686 and R3687 once again provided with a base current.
Transistor 7687 starts conducting and the process is repeated several times (see Fig. 2-14). During non-conductance of TS7687 at the secondary side of transformer 5663 the energy is given by winding 12-13. Contrary to the normal operation of the S.O.P.S. not all energy is transferred to the secondary circuits now. As a result the secondary voltage across winding 12-13 slowly increases. After approx 1 ms and over 20 to 30 pulses the secondary voltage has risen sufficiently (approx 7 V) to bring TS7685 in conductance via the opto-coupler control and to keep it conducting. Via TS7686 TS7687 is kept switched off for some time and the cycle is repeated.

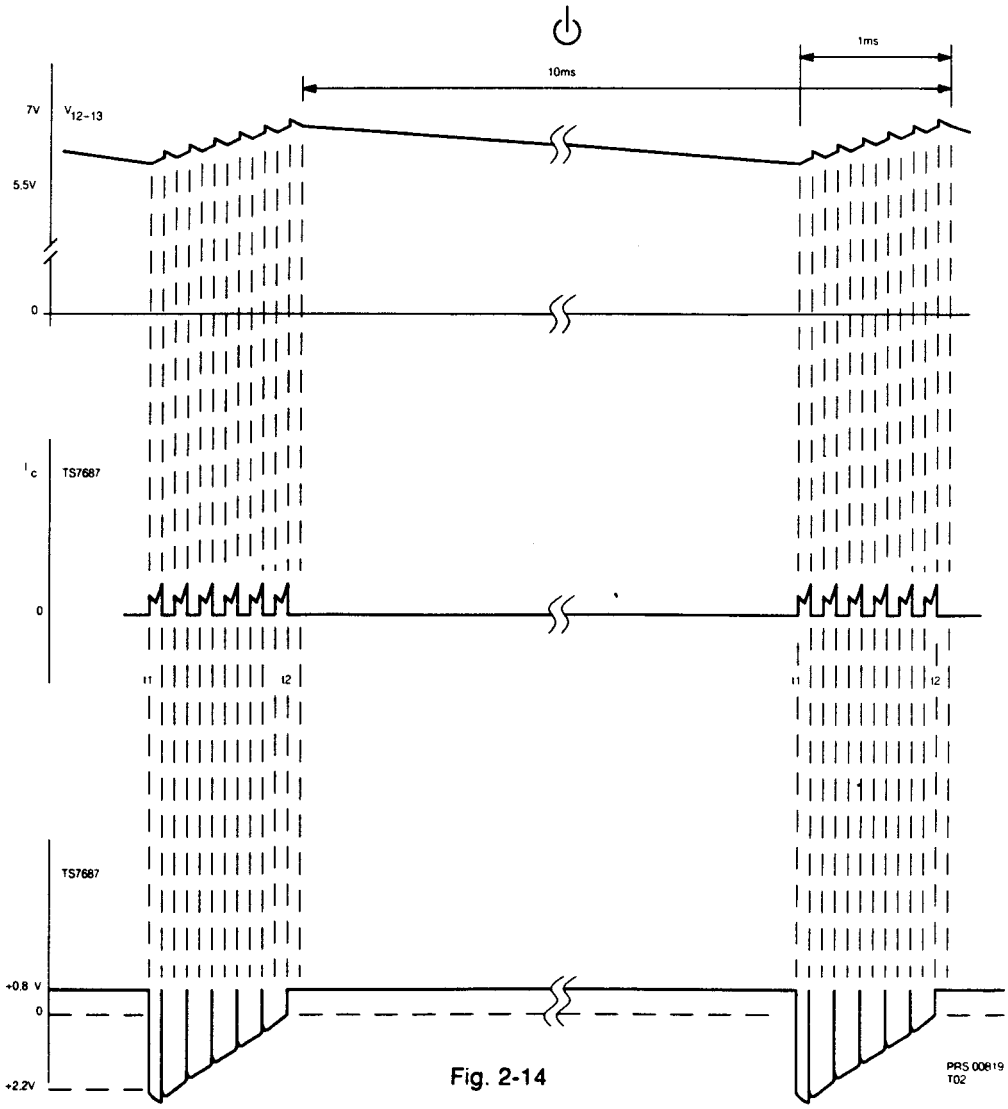


Fig. 2-14

2.4 Automatic degaussing

The circuit for the version with the 90° picture tube is shown in Fig. 2-15. In cold state PTC resistors R3653a and R3653b have a low resistance. Upon switching on of the TV set the current through degaussing coil 5991 is about 5A.
The PTC resistors are warmed up and their resistance value increases very rapidly. As a result the current through degaussing coil 5991 becomes very low (a few mA). Because R3653b is coupled thermally to R3653a, the resistance value remains high and the current low.

The circuit for the version with the 110° picture tube is shown in Fig. 2-16.
NTC resistor R3653b which is coupled thermally to R3653a now sees to it that R3653a is kept warm. To limit the switching-on current, resistor R3653b has been executed as NTC resistor.

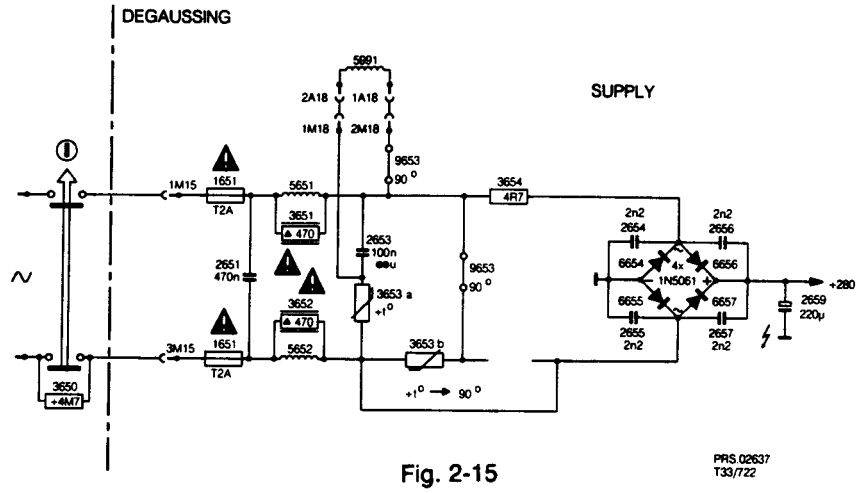


Fig. 2-15

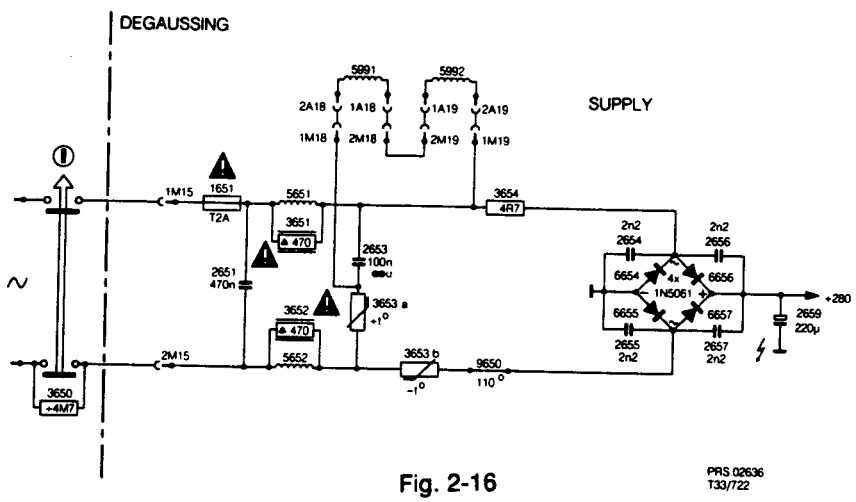


Fig. 2-16

3. THE FRONT-END MODULE

Figure 3-1 gives a block diagram.

3.1 Tuner part

The VHFa bandswitch voltage is applied to pin 7 and the VHFb bandswitch voltage to pin 8. The UHF bandswitch voltage is fed to pin 10.
The tuning of the RF amplifier and the oscillators is determined by the tuning voltage that is fed to pin 11. This tuning voltage can orignate from any control system and is corrected by the AFC voltage.
After mixing of the oscillator and the RF signal the IF signal is formed which is amplified and fed to output.
The AGC voltage at pin 5 controls the amplification of the RF amplifiers.
The oscillator frequency is divided by 256 (called prescaler) and applied to the CITAC circuit via pins 13 and 14.
The divider is fed by a 5 V voltage at pin 12.

3.2 IF-Part

The IF signal coming from the tuner is fed to the SAW filter (surface acoustic wave).

The SAW filter determines the total IF response curve. In this filter the input signal is converted by a transducer into an acoustic signal which is via a ceramic carrier transmitted to a second transducer. This transducer converts the signal again into an electric signal. The form of the ceramic carrier determins the frequency response.

After this SAW filter the IF signal is fed to controlable amplifier "A" in TDA2541. The amplification is determined by IF AGC circuit "B".
After this amplifier the signal is fed to video synchronous demodulator "C" After detection the luminance signal appears with superimposed on it the colour information at 4,43 MHz. Via amplifier "F" this signal is fed to pin 28. Amplifier "F" also contains an inverter against interference voltages which exceed a certain limit. It prevents white dots in the picture and the synchronization is not disturbed.
TDA2541 also contains a second synchronous demodulator "H". The circuit provides an AFC voltage to correct mistuning.
Via the AFC switch circuit "G" the AFC voltage is fed tot pin 23.
The AFC voltage at pin 23 is nominally 6V. If the tuning drifts this voltage will rise or drop. From pin 23 the AFC voltage is fed to the CITAC circuit to correct the tuning.
Block "B" is the IF gain control. Here the peaks of the sync pulses are being detected. They are a measure for the amplitude of the aerial signal. If the aerial sigal becomes greater the IF gain is reduced.

IF the gain has been reduced maximally and if the aerial signal still is too great, the RF-AGC becomes operative.The RF-AGC voltage is fed to the RF-amplifiers at the tuner part.
The point at which the RF-AGC becomes operative is determined with the preset potentiometer connected to block "B".
In the IF-part the quasi split sound principle has been used. For this purpose a separate IF sound circuit with the IC, TDA2545A is used.

From the SAW filter a IF signal has been separated and is fed to the input at the IC, TDA2545A. In the IC the signal is fed to an controlled amplifier with three stages. The amplification is determined by the AGC circuit.
After this amplifier the signal is fed tot a synchronous demodulator. After detection the signal has been amplified and then fed to the output pin 24.
On pin 24 the FM sound signals are also present. (For PAL B/G-H 5,5 + 5,74 MHz and for PAL I 6 MHz).

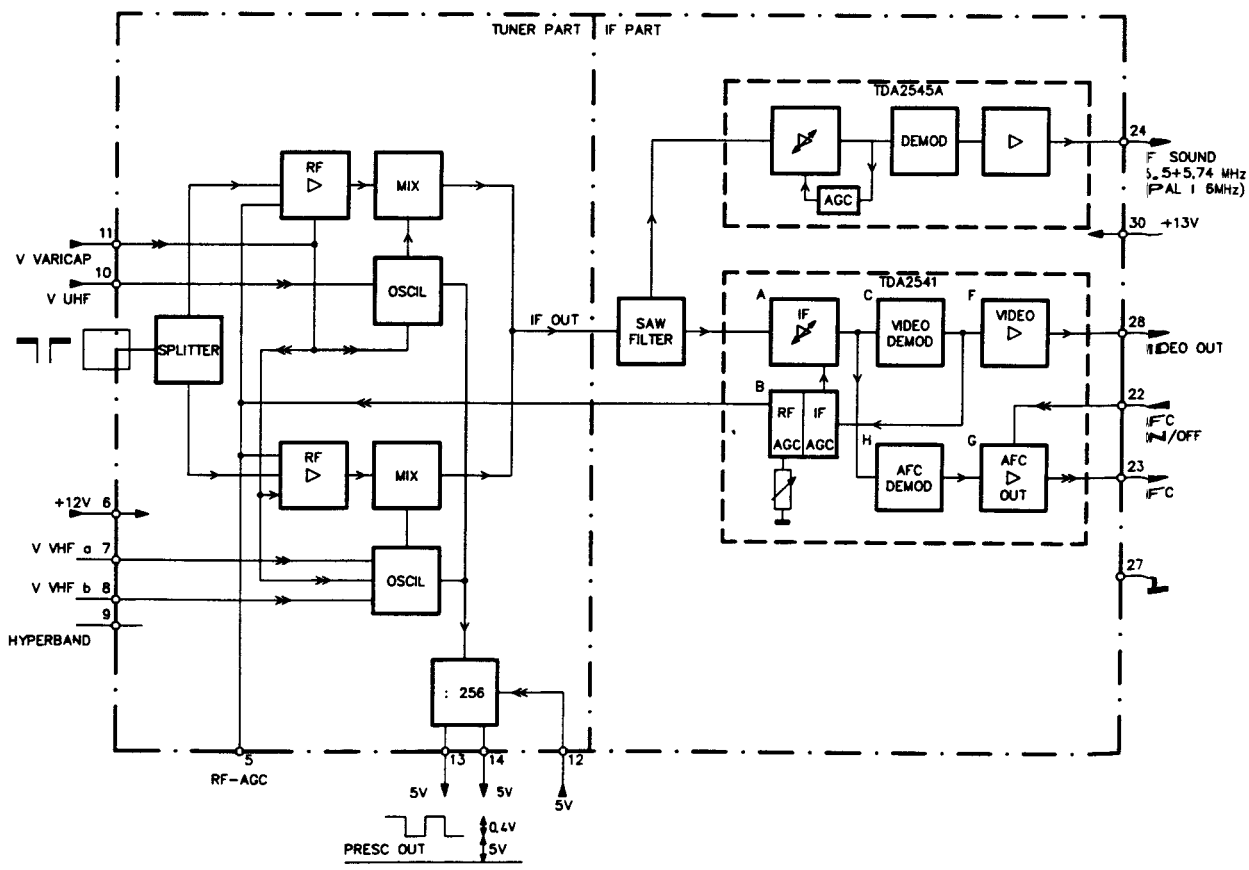


Fig. 3-1

4.1 Luminance filter circuit (Fig. 4-1)

The video signal from IF-detector is fed to pin 15 of IC 7300 via C2251//R3251, luminanc[illegible]lay line 5251, R3252 and C2255. The delay line [illegible]s the time delay of the Y-signal so that the lumina[illegible] and the corresponding chromincance signal are simultaneously present on the video control IC7300.
S5252, C2252 are adjusted to 4,43 MHz to avoid an interference pattern.

4.2 Chrominance circuit (Fig. 4-1)

The video signal is via C2253, C2254, C2259 and the band suppres filter S5250-C2250 (approx 6,5 MHz) fed to pin 9 of IC7250.
Absorption circuit C2258-S5258 is tuned to 2,2 MHz for the following reasons. The mixture in the video synchronous demodulator of IF signals of approx 36,7 MHz with the picture carrier of 38,9 MHz will result in signals of approx 2,2 MHz. The second harmonics of these signals will interfere with the 4,43 MHz chrominance signal. This will result in signals with difference frequencies which will fall in the pass-band of the chrominance demodulator.
On the picture screen they will be visible as annoying interference; the above-mentioned frequencies will thus have to be suppressed.
In the IC the chroma signal is amplified, C2262 is a decoupling for the DC negative feedback. The amplification is controlled by the chroma AGC, C2261 and C2263 are the detector capacitors.

- The chroma signal is separated from the burst signal and goes to an output amplifier which controls the delay line. The signal also goes directly (inside the IC) to the matrix circuit.

- The phase of the [illegible]d signal is adjusted with S5267 and S5268 [illegible]mplitude is matched with R3268 to that of the direct signal.

- The sum of the direct and the delayed signal gives us the
  +(B-Y) component.
  The difference of the direct and the delayed signal gives us the R-Y component which is positive for a +(R-Y) line and negative for a -(R-Y) line.

- The burst signal goes to the burst demodulator where the phase of the burst signal is compared in phase with the +(R-Y) reference signal.
  The flywheel effect is obtained with C2274, C2273, R3274 and R3273. If pin 11 is connected to ground, the oscillator is not synchronised and the free running can be adjusted with C2272. The phase discriminator controls the PAL oscillator. This 8.86 MHz oscillator is a crystal oscillator. After a 2:divider we obtain 2 signals that have shifted 90° in phase and that are used as R-Y and B-Y reference signals for the demodulators. The R-Y reference signal is every other line shifted 180° controlled by the PAL flip flop. This FF is compared with the demodulated burst and if necessary corrected so that for a +(R-Y) line the reference signal is shifted 0° and for a -(R-Y) line 180°.

- The 2 synchronous demodulators give a -(R-Y) and a -(B-Y) signal to the outputs.

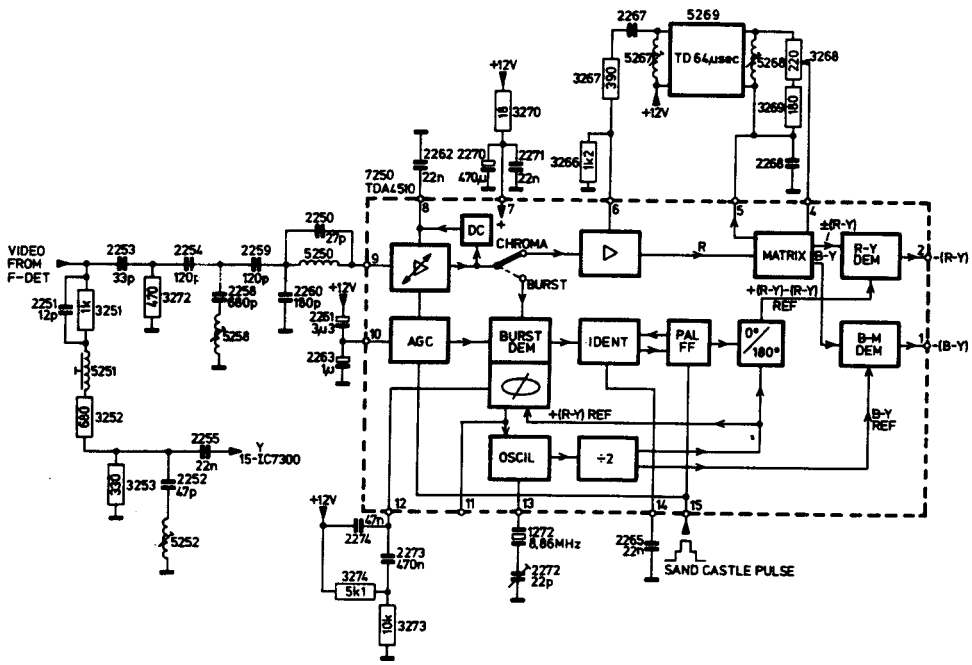


Fig. 4-1

42 230 B12

5. VIDEO CONTROL (see fig. 5-1)

5.1 Introduction.

- The video control IC TDA 4580 receives input signals from 3 different sources:
  . chroma module : y signal, – (R–Y) and –(B–Y)
  . SCART : R, G and B signal + RGB blanking
  . TXT : R, G and B signal + TXT blanking.

- The signals from the chroma module and from the Scart can be adjusted in luminance, saturation and contrast.
  TXT signals can only be adjusted in luminance.

- A beam current limiter and a cut–off point stabilisation are present.

- The output signals are RGB.

5.2 TDA 4580.

If the voltage at pin 11 is low (less than 0,4 V), the TV signals Y, –(R–Y) and –(B–Y) are passed on. A high voltage (more than 0,9 V) at pin 11 swithces on the Scart signals. These RGB signals are converted into Y, –(R–Y) and –(B–Y) in the following way. An opamp receives the RGB signals as input signals.
The R–signal appears at R 1, it has been selected so that the amplification for R = 0,3 X; R2 and R3 take care for an amplification of 0,59 and 0,11 for G and B respectively.

After an inverter we obtain the Y–signal.

Op–amp B and C add the R of B signal to the –Y–signal. This signal is inverted so that we obtain –(R–Y) and –(B–Y).

- The 3 signals coming from SCART or from chroma each pass through an adjustable amplifier. The saturation controls the amplification of the colour difference signals and with the contrast the y–signal and the colour difference signals are controlled.

- The luminance control controls the backporch level of the y–signal.

- A matrix circuit first makes the G–Y signal and adds the y–signal to the colour difference signals so that RGB signals are obtained.

- A second switch is controlled with the TXT blanking (fast blanking) and switches on the TXT signals if pin 28 is high (greater than 0,9V). The TXT signals are clamped at the same black level as the RGB signals of the matrix. The TXT signals have the same luminance and are thus controlled together with the luminance control.

- Via the cut–off point stabilisation (that will be discussed later) the RGB signals come out of the IC on the pins 1, 3 and 5.

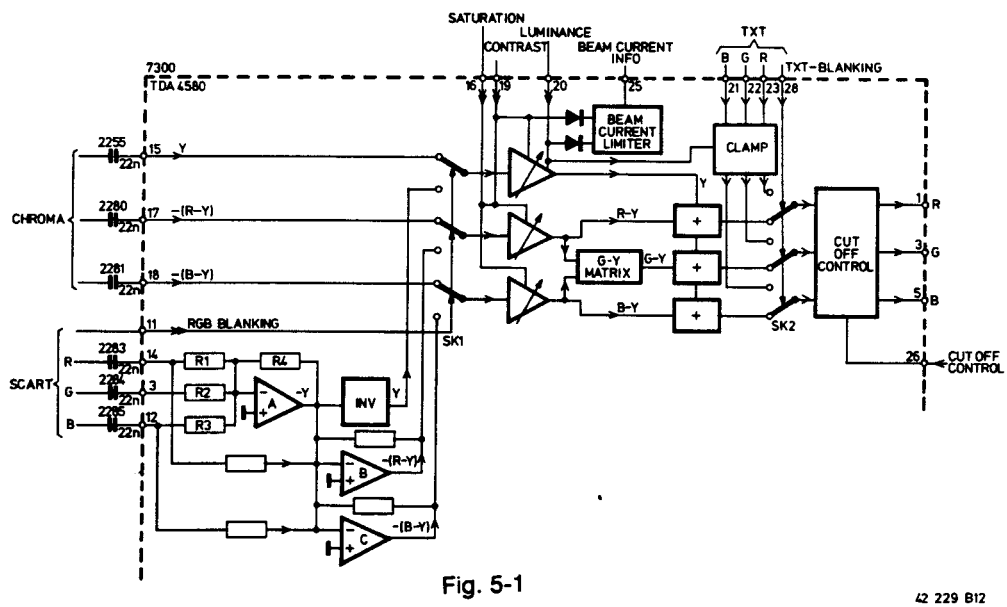


Fig. 5-1

42 229 B12

6. RGB AMPLIFIERS.

The R, G and B amplifiers are all identical. That is why only the G amplifier will be described (see fig. 6–1).
The base voltage of TS7465 is adjusted for 3 V, the emitter voltage is 3.7 V and is used as reference voltage for the 3 amplifiers.

6.1 DC adjustment at black level.

The cut–off point stabilisation in IC7300 adjusts the black level for approx 1,5 V. After R3434 this black level lies at 2,25 V. The amplifier with TS7432, TS7433 and TS7422 can be seen as op–amp. b–TS7432 is – input, e–TS7433 is + input, both are at 3,7 V.
The voltage across R 3428 + R3429 = 3,7 – 2,25 = 1,45 Volts.

The current through

$$R3428 + R3429 = \frac{1{,}45 \text{ Volts}}{1\text{ K }5 + 470\text{ E}} = 0{,}725 \text{ mA}$$

$$\text{The current through R3430} = \frac{3{,}7 \text{ Volts}}{2 \text{ K}} = 1{,}85 \text{ mA}$$

The current through R 3427 and R3426 is the sum of those two currents, so 1,85 mA + 0,725 mA = 2,575 mA
This gives a voltage across R3427 and R3426 of
2,575mA x 66 K = 170 V.
So that V out = 170 + 3,7 = 173,7 Volts

6.2 Amplification

$$G = \frac{R3426 + R3427}{R3428 + R3429} = \frac{66 \text{ K}}{2\text{K}} = 33 \text{ X}$$

6.3 DC setting

At DC a constant current is flowing through TS7422
The voltage across

$$R3421 = \frac{200 \text{ Volts} - 12 \text{ Volts}}{180 \text{ K} + 6 \text{ K2}} \text{ x } 6\text{K2} = 6{,}2 \text{ Volts}$$

The voltage across

R3422 = 6,2 Volts – 0,7 Volts = 5,5 Volts,
this gives a current through R3422 of

$$\frac{5{,}5 \text{ Volts}}{2 \text{ K}} = 2{,}7 \text{ mA}$$

The signal of the b–TS7433 appears at b–TS7422 via C2423. C2422 decouples the emitter which results in a great gain.

The output signal appaers via 2 emitter followers TS7480 and TS7438 at the cathode of the picture tube. The beam current flows via TS7480 through R3481, which gives a voltage for the cut–off point stabilisation. With positive voltage jumps TS7438 starts to conduct and quickly charges the parasitic capacitances.
The B–amplifier is identical with the G–amplifier. The R–amplifier has a fixed voltage division instead of potentiometer R3434. The gain of green and blue is adjusted relative to the gain of red. This is white–D adjustment.

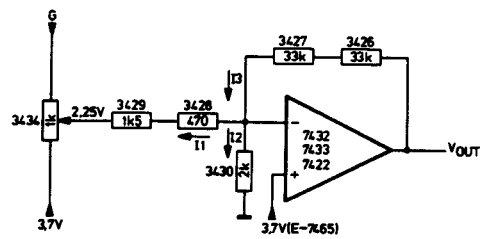


Fig. 6-2

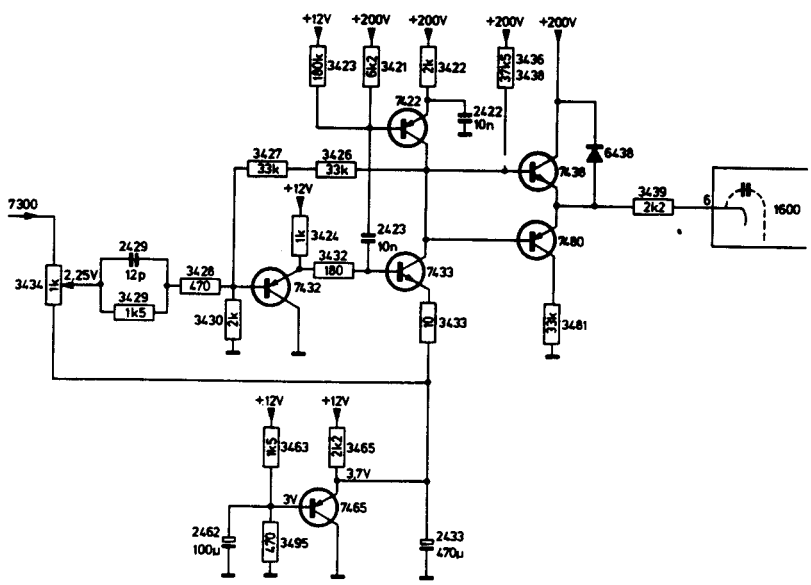


Fig. 6-1

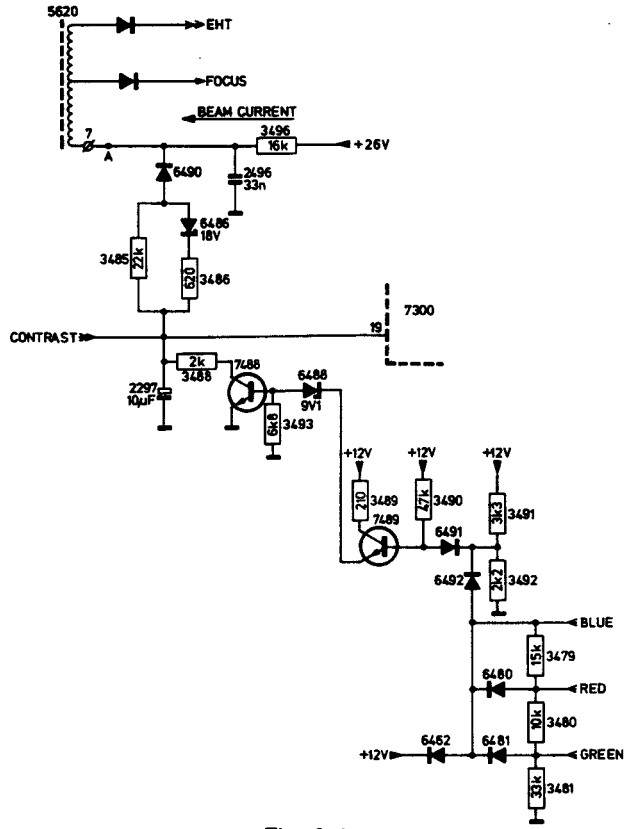

5620
EHT
FOCUS
BEAM CURRENT
3496
16k
+26V
7
A
6490
2496
33n
6486
18V
3485
22k
620
3486
7300
19
CONTRAST
2k
3488
7488
6488
9V1
2297
10µF
6k8
3493
+12V
+12V
+12V
210
3489
7489
47k
3490
3k3
3491
6491
6492
2k2
3492
BLUE
15k
3479
6480
RED
10k
3480
6482
6481
+12V
GREEN
33k
3481
42 211 B12

Fig. 6-4

6.4 Cut–off point stabilisation (see fig. 6–3)

During frame flyback the picture is blanked. There always is a small leakage current flowing, it flows through R3479, R3480 and R3481. The voltage measured across these 3 resistors appears at IC7300 point 26. During the 10th to the 13th line a pulse generator closes switch SK and this voltage is stored in C2289 and will then be the reference voltage for the 3 cut–off point stabilisations.
On the 23rd line the pulse generator adds a pulse to the R–signal on the 24th line to the G–signal and on the 25th line to the B signal. These pulses cause a minor beam current.
With the same beam current the red, green and blue phosphor dots will give a different luminance. To cut–off the picture tube correctly the green beam current only flows through R3481, the red one through R3480 and R3481 and the blue one through R3479, R3480 and R3481. Further we will see that the measured voltage is stablized at 0,5 V so that the cut–off current will be:

$$G = \frac{0{,}5 \text{ Volts}}{33 \text{ K}} = 15\ \mu A$$

$$R = \frac{0{,}5 \text{ Volts}}{43 \text{ K}} = 12\ \mu A$$

$$B = \frac{0{,}5 \text{ Volts}}{58 \text{ K}} = 8{,}5\ \mu A$$

The pulse that enters at pin 26 of IC7300 thus comprises apart from the leakage current information also 3 positive beam current pulses, namely the 23rd line for R, the 24th line for G and the 25th line for B. The pulse generator causes a switch to close so that during the 23rd line this signal appears at the – input of the comparator.
It compares the pulse with a voltage that is 0,5 V higher than the leakage current voltage. The comparator gives a voltage that is saved for the next frame by C2300 and gives a DC voltage to the R–signal.
This signal comes out at pin 1 and is via the R–amplifier sent to the picture tube.
If the cut–off voltage for red is too high, the beam current for red rises and the pulse too c[illegible]ng line 23. The comparator gives a low voltage and C23[illegible]0 discharges until the beam current of red gives a voltage drop of 0,5 Volts across R3481 during line 23. During line 24 the green amplifier is driven and during line 25 the blue amplifier. The DC voltage for green is stored in C2301 and for blue in C2302.
D7462 ensures that in case of a great beam current the voltage at pin 26 of IC7300 does not exceed 12,7 Volts. In case of flash–over the great current also flows away through D7462.

6.5 Beam curent limiter (see fig. 6–4)

The beam current flows through R3496, the voltage at point A is used to limit the maximum beam current. In case of black picture (beam curent = 0) the voltage at A equals 22 Volts. The 4V voltage drop is caused by the current through the focussing pot. With high luminance the voltage drops to below the contrast voltage. D6490 conducts and via R3485 the contrast voltage is decreased and the beam current drops.
In case of fast luminance changes (white lines) D6486 shows the Zener effect and via R3486, C2297 is discharged quickly.

The beam current of green flows through R3481, of red through R3480 and R3481 and of blue through R3479, R3480 and R3481. The voltage at the cathode of D6492 is determined at 4,8V by R3491 and R3492. As soon as the voltage at the anode of D6492 (sum of the 3 beam currents) becomes greater than 5,5 Volts, D6492 conducts. Normally D6491 is conducting, so that the voltage at the base of TS7489 is the same as at the anode of D6492. If the voltage at the emitter of TS7489 becomes greater than 9,1 Volts D6488 and TS7488 conduct thus reducing the contrast.
D6462 ensures that the voltage does not exceed 12,6 Volts and protects the circuit against high–voltage flash–over.
In case of fast changes the g1–cathode capacitances of the picture tube discharges and we obtain an additional current peak. The resultant voltage peak causes D6491 to block for a moment until R3490 has recharged the b–e capacitance of TS7489.

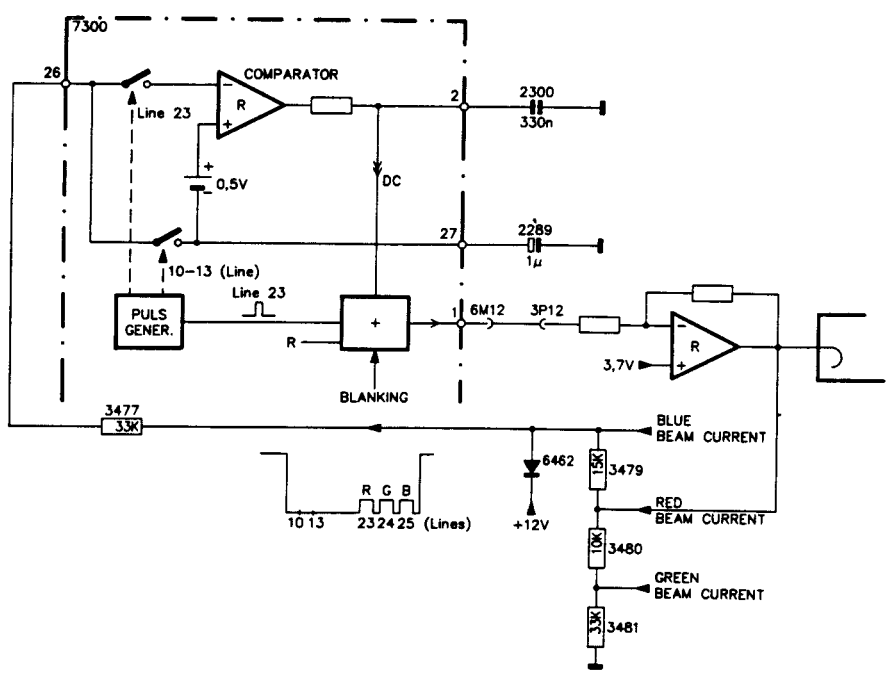


Fig. 6-3

7. SOUND PATH

7.1 Block diagram (see fig. 7-1)

The stereo decoder has been executed as module.
IC 7102 and IC7108 demodulate the 5,5 and 5,74 MHz sound signal.
In IC7125 the matrix and the identification can be found.

IC7137 switches on sound of scart or of front-end. In IC7145 the selection is made between stereo, spatial stereo, spatial mono or mono.
Switching over to these systems is done by 2 ICs, namely IC7134 and IC7133.
IC7170 controls volume, treble and bass.
The stereo output amplifier has been mounted on the mono carrier and consists of 2 ICs, namely IC7220 and IC7210.

7.2 The demodulators (see fig. 7-2)

The sound signal goes to 2 demodulators (IC7102, IC7108) via a circuit tuned to 5,5 and 5,74 MHz respectively. These circuits consist of coils S5100/S5101 tuned to 5,5 MHz and S5106/S5107 tuned to 5,74 MHz.
IC7102 demodulates the 5,5 MHz. The AF signal (mono or 1st language) is via R3111 passed on to the matrix.
IC7108 demodulates the 5,74 MHz. It contains apart from the 2x right signal or 2nd language also the identification signal.
With R3111 we can adjust the 2 output signals for an equal amplitude.

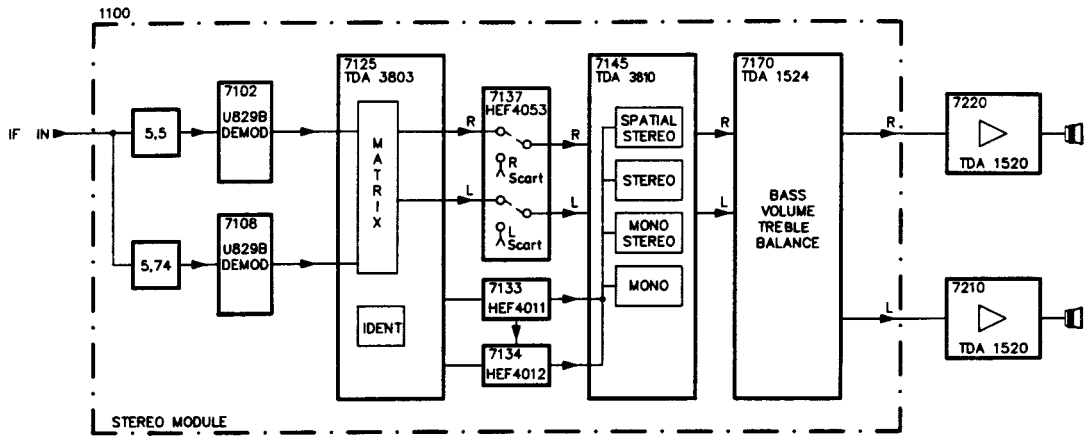
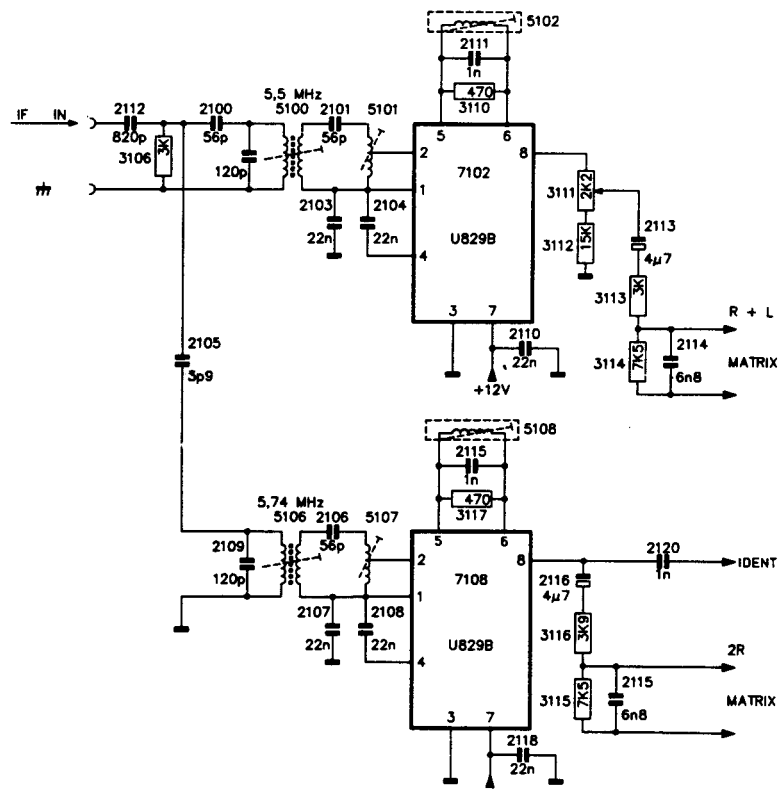


Fig. 7-1

42 240 81



7.3 The stereo matrix (see fig. 7–3)

The stereo matrix is situated in IC7125 (TDA3803).
The IC receives the following signals.

MONO	pin 25	mono signal
	pin 27	no signal
STEREO	pin 25	R + L
	pin 27	R
DUAL SOUND	pin 25	1st language
	pin 27	2nd language

The matrix is formed by 3 op–amps. Let us examine the outputs for these 3 cases.

- Mono
  Via op–amp I the mono signal is passed on and on the output of op–amp I the – (L + R) signal appears.
  Op–amp II receives no input signal.
  Op–amp III receives the –(R + L) signal at its + input so that it gives –(R + L) at its output.

- Stereo
  Op–amp I gives –(R + L) at its output.
  Op–amp II gives "– R" while op–amp III gives "– L".

- Dual sound
  Op–amp I gives as output the 1st language while op–amp II passes on the 2nd language.

We thus obtain for the 3 cases the different signals (mono/stereo/1st, 2nd language) at the output of the matrix. They go to a switching unit where they are switched on to the outputs. C2114, C2115 see to deemphasis.

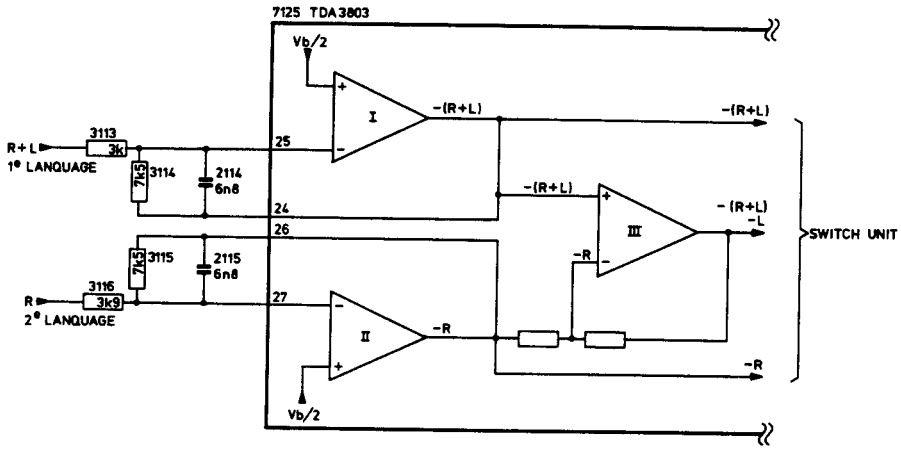


Fig. 7-3

42 209 B12

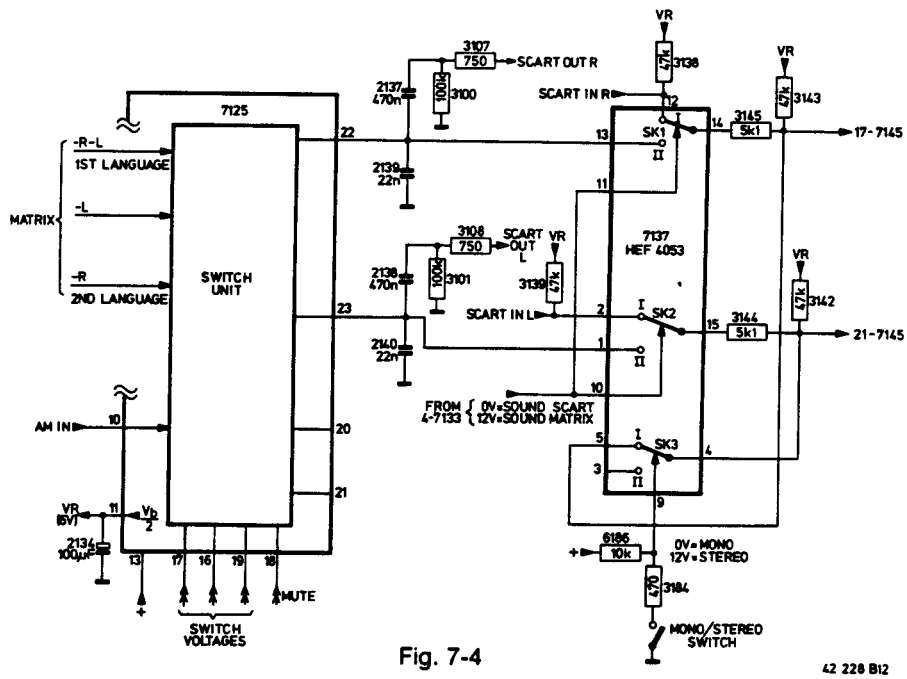


Fig. 7-4

42 228 B12

7.4 The switching unit (see fig. 7–4)

The switching unit is also situated in IC7125. It contains a number of switches that send the correct signals to the outputs. The IC has 4 outputs that are switched by pins 17/16 and 19.
Below follows a table of the mode of these switches and the switched signals.
With a multi set an AM signal can be injected at pin 10 of IC7125. For, if pin 18 is rendered high, all output signals of the matrix are interrupted. If a signal is applied to pin 10 then, it is passed on to outputs 23 and 22 of IC7125.
Between IC7125 and IC7145 switching IC7137 is situated. This IC contains 3 double–throw switches. SK 1 and SK 2 switch on the signal of IC7125 or of the scart connector. The mode of the switches is determined by the external function (switched on by RC5 transmitter of via scart).
The 3rd switch SK 3 is switched by the mono/stereo switch. If the mono switch is depressed, pin 9 of IC7137 is at 0V. Then the left–hand and right–hand signals are interconnected via SK 3.
Via C2137 and C2138 the right–hand and left–hand signals are branched off and brought to the scart output.

7.5 Switching over sound with scart (see fig. 7–4)

With SCART a high voltage is presented to IC7133 via the key "extern". This IC converts this voltage in a voltage of 0 Volts at pins 10 and 11 of IC7137. As a result SK 1 and SK 2 assume the I mode. The sound of scart enters at pins 12 and 2 of IC7137 and is by SK 1 and SK 2 switched on to pins 14 and 15 of IC7137.

IC7125 receives supply voltage at pin 13 of IC7125. This voltage is 12 Volts and is supplied by the line output stage. In the IC a reference voltage is made which comes out at pin 11. This voltage equals 6 Volts.

7.6 The identification circuit (see fig. 7–5)

The identification circuit is also situated in IC7125. To pin 2 of IC7125, in case of stereo and 2–language broadcasts, an AM modulated signal is applied with 54,6 kHz as carrier. This carrier has been modulated with 117,5 Hz for stereo broadcasts and with 274 Hz for 2–language broadcasts. This signal is present on the R–signal which contains either the 2nd sound carrier for stereo or the 2nd language for bilingual broadcasts.
To seperate these 2 we send these signals through an amplifer that is tuned to 54,6 kHz. The tuned circuit is situated at pin 1 of IC7125 and consists of S5134/C2141. At the output of this amplifier (pin 1) we thus find only the modulated 54,6 kHz signal. We will demodulate this signal in an AM detector. At pin 28 of IC7125 we find the 117,5 Hz or 274 Hz AF signal.
This signal goes to 2 op–amps that are both switched as a tuned amplifier. One is tuned to 117,5 Hz and the other to 274 Hz.

The outputs of these selective amplifiers are now detected in an identification circuit. Capacitors C2135/C2136 form the detection capacitors. This identification circuit also drives via the pins 14 and 15 the LEDs for language I or II indication or stereo.

Pin	High	Low	.23/.22	.20/.21
19	X or open		stereo	stereo
19		X	mono	mono
16	X			1st language
16		X		2nd language
17	X		2nd language	
17		X	1st language	

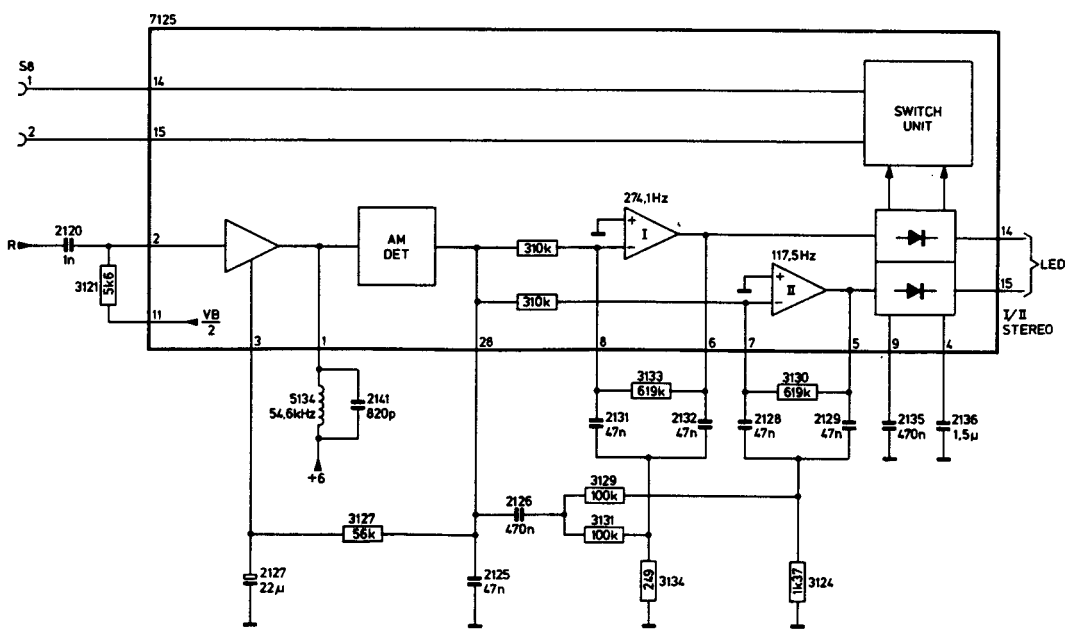


Fig. 7-5

42 227 B12

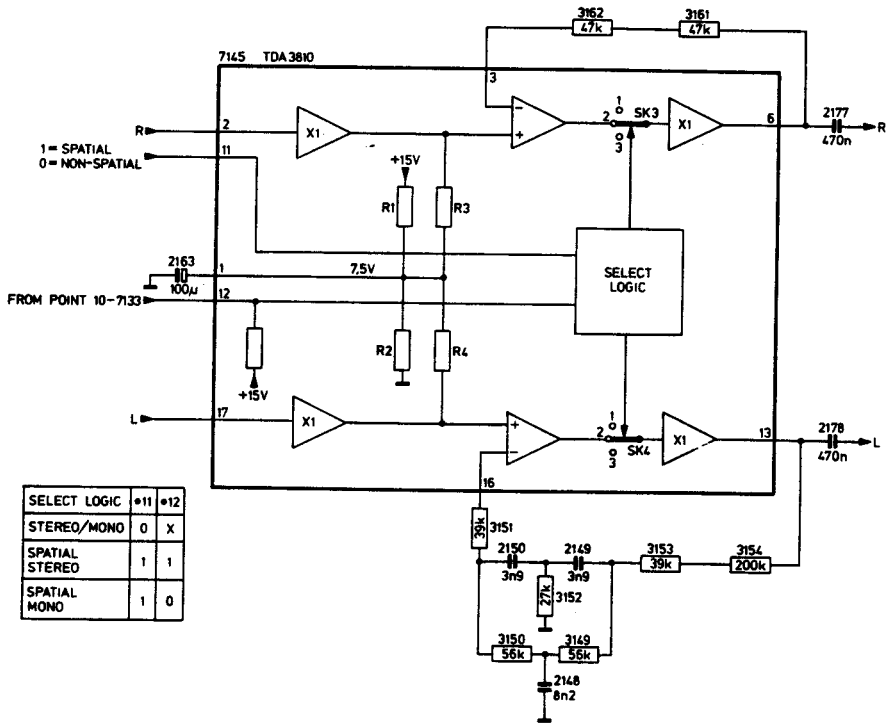
7.7 TDA 3810.

Via the control panel logics TDA 3810 can be switched in 3 modes, viz. stereo/mono, spatial stereo and spatial mono.

7.7.1 Stereo–mono (see fig. 7–6)

In the stereo mode the logics keep pin 12 of IC7145 high. Pin 11 is kept low by the control (mode not spatial). In the IC switches SK 3 and SK 4 will be in mode 2. The left–hand and the right–hand signals are sent through 3 amplifiers with a gain equal to 1.

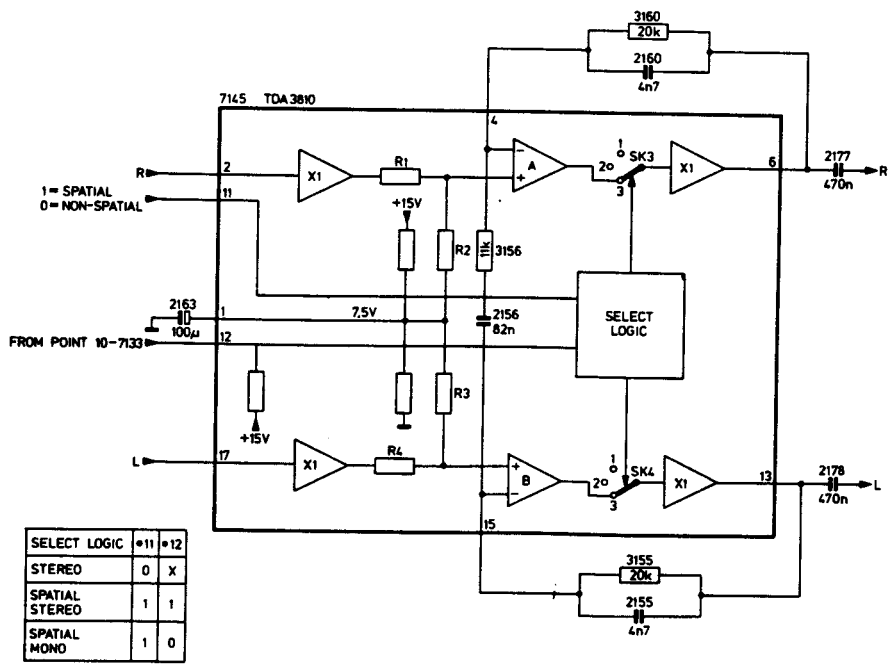
At pin 6 and pin 13 these signals come out, R3162 and R3161 form the negative feedback resistors in the right–hand channel. This negative feedback ensures that the output voltage is kept at 7,5 Volts (+ input is also kept at 7,5 V within the IC).
In the left–hand channel the negative feedback is formed by R3151, R3150, R3149, R3153 and R3154. Capacitors C2150 and C2149 have no effect at all here.
In the mono mode left and right are identical, but the IC remains in the stereo mode.



SELECT LOGIC	•11	•12
STEREO/MONO	0	X
SPATIAL STEREO	1	1
SPATIAL MONO	1	0

Fig. 7-6

42 226 B12



SELECT LOGIC	•11	•12
STEREO	0	X
SPATIAL STEREO	1	1
SPATIAL MONO	1	0

Fig. 7-7

42 224 B12

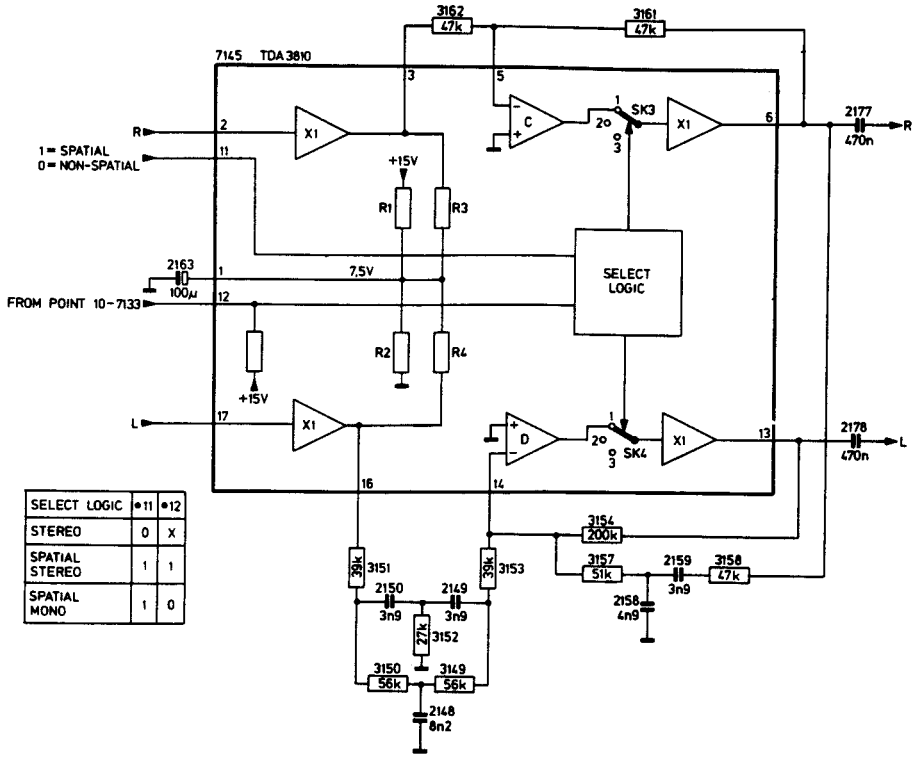


Fig. 7-10

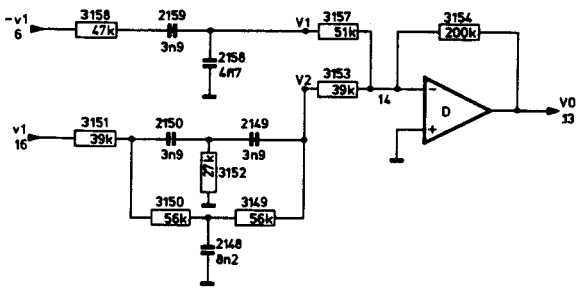


Fig. 7-11 42 202 A12

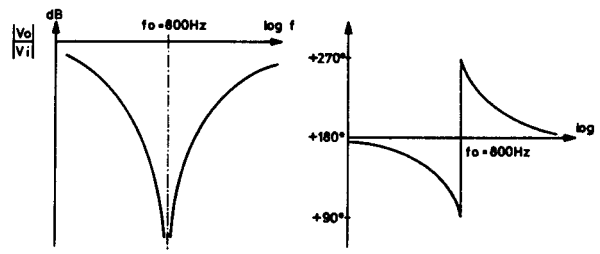


Fig. 7-13 42 204 A12

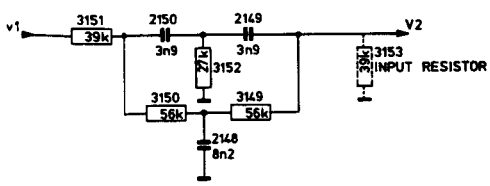


Fig. 7-12 42 203 A12

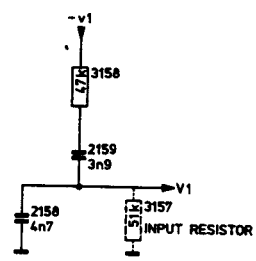


Fig. 7-14 42 205 A12

7.7.2 Spatial on stereo (see fig. 7–7)

In the stereo mode pin 12 of IC7145 is high.
Pin 11 of IC7145 is high (because spatial is desired) so that switches SK 3, SK 4 are in mode 3.
Here we get 2 amplifiers of which the gain equals in both cases.

$$\frac{R3155 \,//\, X\,C2155 + R3156 + X\,C2156}{R3156 + X\,C2156}$$

The + input of both amplifiers apparently is ground for AC voltage (via R 2, C2163 and R 3, C2163.).
We also see that the two "–" inputs are interconnected via R3156, C2156.
Let us examine op–amp B and assume that no signal enters at the right.
This will result in the frequeny response accordingly to Fig. 7–8

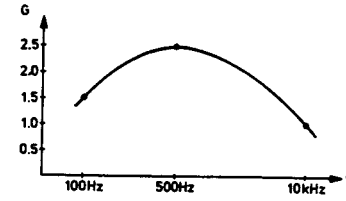


Fig. 7-8 42 200 A12

For low tones: impedance C2156, R3156 is great. the gain is slightly greater than 1.

For middle tones: impedance C2156 has dropped. the gain has become greater the max. lies at approx 500 Hz.

For high tones: the impedance of C2155 drops and thus the gain drops again.

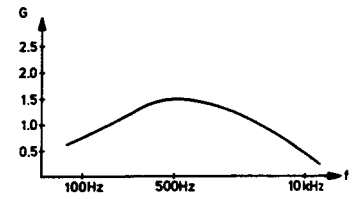


Fig. 7-9 42 201 A12

The input signal for op–amp A is the signal that is present at the + input of op–amp B. R3156, C2156 now becomes the input resistance and C2160/R3160 the negative feedback resistance. The gain now equals:

$$\frac{R3160 \,//X\,C2160}{R3156 + X\,C2156}$$

Since R3156 + C2156 here function as input resistance the gain will be less, but the frequency response (see fig. 7–9) equals that of op–amp B.

Since the signal appears at the – input of op–amp A the signal will be inverted.
On the left–hand output we thus obtain the amplified left–hand signal with some attenuated treble and bass.
On the right–hand output we thus obtain attenuated left–hand signal, of which mainly the middle notes are received. When we repeat this reasoning with only a signal at the right–hand input and no signal at the left–hand input, we obtain at the right the right–hand signal and at the left the attenuated right–hand signal.
This lends the stereo signal the spatial effect.
Since something is added to the right–hand signal (–L) and (–R) is added to the left–hand signal, the signal will first be attenuated with R1/R2 for the right and with R3/R4 for the left.

With a mono signal L = R, across R3156,C2156 there is no voltage difference and thus no current flow. Both op–amps amplify 1 x. Because of the attenuation beforehand the mono signal is reproduced weaker.

7.7.3 Spatial on mono (see fig. 7–10)

In the spatial on mono mode pin 11 is high (spatial) and pin 12 low (mono).
As a result SK 3 and SK 4 assume mode 1.
At pin 2 and pin 17 of IC7145 the same signal enters.

If we examine amplifier C, we see that the gain is determined by R3142 and R3161.

$$-\frac{47K}{47K} = -1$$

The gain is independent of the frequency.

Concretely:
the signal that enters at pin 2 of IC7145 (Vi) appears equally great and shifted 180° at pin 6 of IC7145 (–Vi)

If we examine amplifier D(see fig. 7–11), we recognize an adder circuit.

$$V\,0 = -\left[V1.\frac{R3154}{R3157} + V2.\frac{R3154}{R3153}\right]$$

$$V\,0 = -\,[4.V\,1 + 5.\,V\,2]$$

Output voltage V 0 is frequency–dependent here since V1 and V2 are frequency–dependent.
V 2 is determined by the "double–T" filter of fig. 7–12. The playback characteristic and the phase characteristic are shown in fig. 7–13.
V 1 is determined by the circuit from 7–14. The playback characteristic and the phase characteristic are shown in fig. 715.

This results in the following situation (see fig. 7–10):

- At pin 6 of IC7145 appears the input signal shifted 180° (–Vi). This signal goes through filter R3158, C2159, C2158, R3157 to op–amp D which amplifies it 4 x and shifts it another 180°. This implies that we find at pin 13 the playback characteristic of the filter amplified 4 x and that the phase characteristic equals that of the filter.

- At pin 16 of IC7145 we obtain input signal Vi. This signal passes through the "double T" filter and via pin 14 to op–amp D which amplifies it 5 x and shifts it 180° in phase. At pin 13 we thus find the playback characteristic of the "double T" filter amplified 5 x and, moreover, shifted 180° relative to the phase of the "double T" filter.

Together this yields figure 7–16.

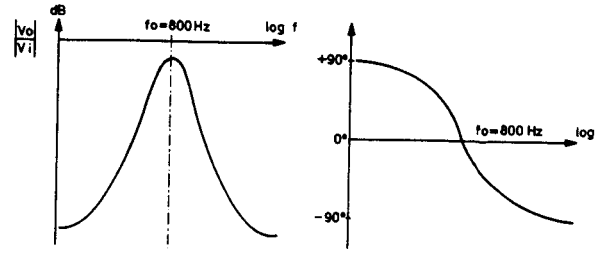


Fig. 7-15

42 206 A12

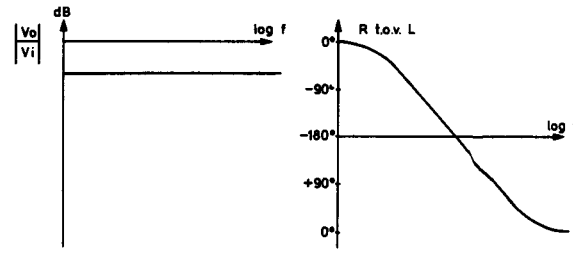
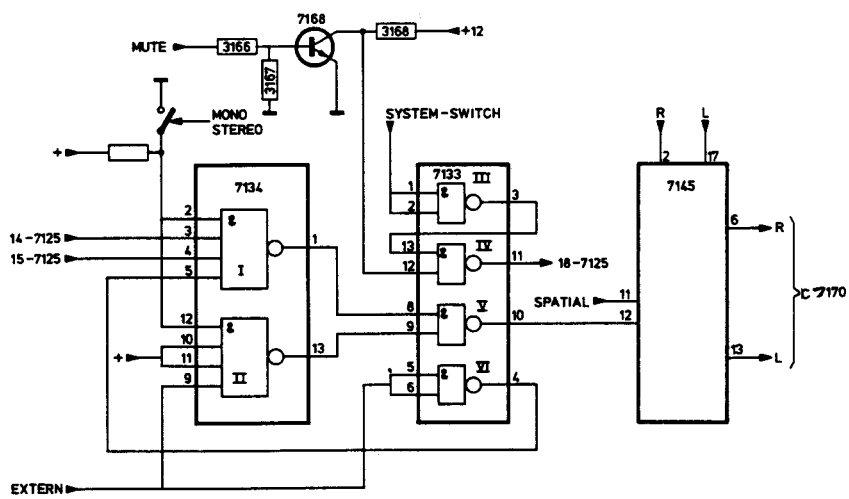


Fig. 7-16

42 207 A12



SELECT LOGIC	•11	•12
STEREO	0	X
SPATIAL STEREO	1	1
SPATIAL MONO	1	0

Fig. 7-17

42 210 B12

We see that the amplitude both at left and at right remains constant as a function of the frequency. The phase, however, varies strongly (0°.....360°) as a function of the frequency.
By rendering the phase shift between the 2 loudspeakers frequency–dependent a spatial effect on mono is obtained.

7.8 Driver stage for IC7145 (see fig. 7–17)

- IC7145 receives L and R signal of the stereo decoder and sends these signals to control amplifier IC7170. According to the voltage at pins 11 and 12 these signals are processed.

  Pin 11 is the spatial input and is directly connected to the CITAC IC of the control
  Pin 12 is switched by IC7134 and IC7133 and, if pin 11 is high, determines whether switching to spatial stereo or to spatial mono.

- TV mode.
  Extern will be low then so that the output of nand II is high. Via inverter (nand VI) pin 5 nand I is high. If pin 14 and pin 15 of IC7125 are high (these are the stereo LED outputs, both are high in stereo mode) and the stereo–mono switch is not operated, the output of nand I is low. The output of nand V will be high too then and spatial on stereo is switched on.
  With mono broadcast, 1st of 2nd language or operation of stereo–mono switch the output of nand I is high; the output of nand V is low then and spatial on mono is switched on.

- EXTERN mode.
  Extern will be high then so that via inverter (nand VI) pin 5 of nand I is low. As a result output of nand I is high.
  Nand II is only operated by the stereo–mono switch.
  On stereo the output of nand II is low and the output of nand V is high so that spatial on stereo is switched on.
  In the mono mode of the stereo–mono switch spatial on mono is switched on.

- Operation of the system key.
  When the system key is operated, the output of nand III is low, thus rendering the output of nand IV high. As a result pin 18 of IC7125 goes high so that AM sound can be injected at pin 19 of IC7125.

- In case of noise.
  If there is no aerial signal, the sync IC will give a high voltage. TS7168 conducts and pin 12 of nand IV goes low, as a result the output 11 of nand IV goes high thus suppressing the sound.

7.9 Controlled amplifier TDA1524 (see fig. 7–18)

In this IC volume, treble, bass and balance are controlled. The signals enter at pins 4 and 15 of IC7170.
The volume control voltage appears at pin 1 of the IC and varies between 1 and 3,5 Volts.
The balance control voltage appears at pin 16 of C7170 and controls from 1 to 4 Volts.

The bass control is determined by the value of capacitors C2190 and C2194, while the treble control is determined by C2181 and C2180.

A DC feedback network between pin 11 and pin 13 determines the control level.
This network consists of R3195 / R3194 / C2195. C2195 ensures that only a DC feedback exists. The voltage at pin 17 of the IC is via a zener clamped to 5 Volts. This switches on a contour control in the IC which ensures that the basses are raised in case of low volume.

This signal appears at pin 8 and pin 11 and is passed on to the output amplifiers.

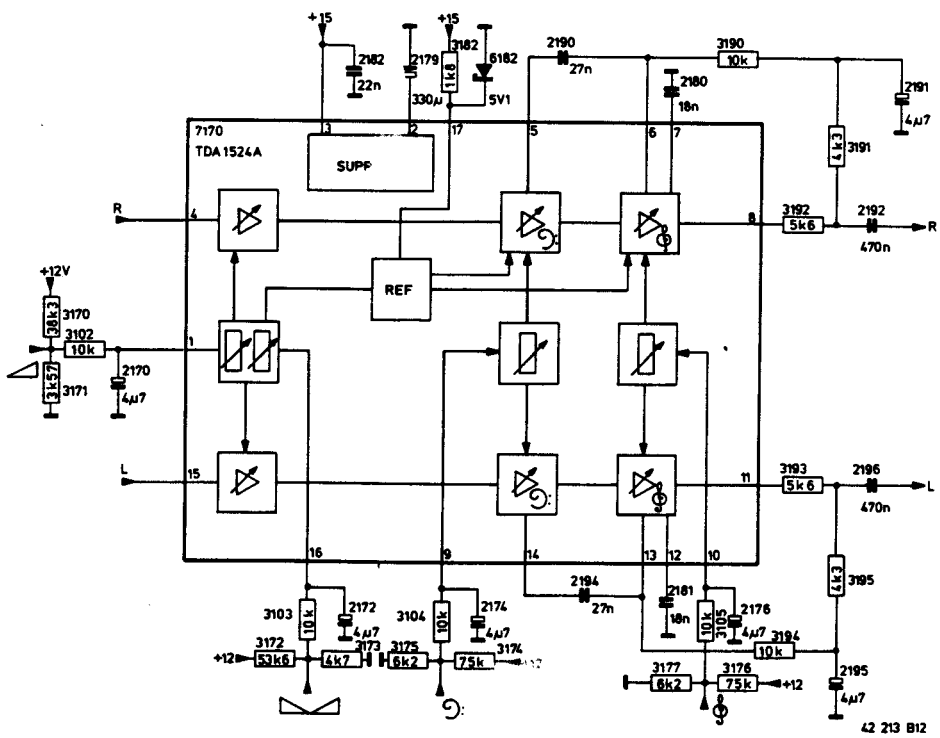


Fig. 7-18

7.10 The output amplifiers.

The two output amplifiers are identical. That is why only the R output amplifier will be described (see fig. 7–19).

The output amplifier is formed by a TDA1520.
The supply voltages are + 20 Volts at pins 6 and 8 and – 20 Volts at pins 2 and 4. The output of the op–amp lies via the loudspeaker at 0 V. Because of the feedback resistor R3204, 0 V is present at the + and the – input.
In the AC field the negative feedback is determined by R3205 and R3204.
The gain equals:

$$\frac{R3204 + R3205}{R3205} = \frac{22\ K + 1\ K\ 3}{1\ K\ 3} = 18 \text{ times}$$

C2200 sees to decoupling of the amplifier for very high frequencies (above the audible range).
R3203 / C2203 form the boucherot filter.
R3201 / C2202 ensure that the IC will not oscillate for certain frequencies.

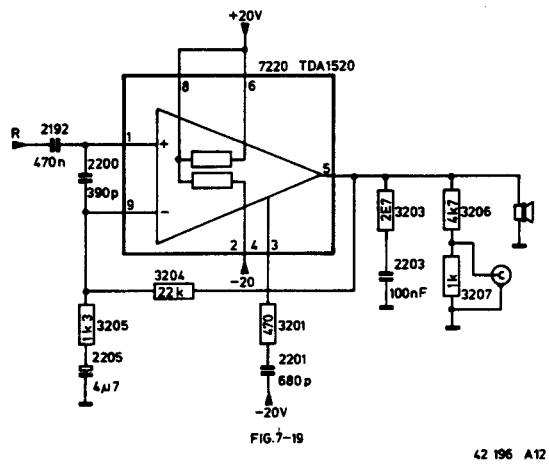


Fig. 7-19

8. SYNCHRONIZATION CIRCUIT

8.1 Block diagram (see fig. 8–1)

The video signal of front–end and scart enters at pins 1 and 5 of the sync IC. A video switch chooses between the two signals, the selector is driven by operation via I^2C bus. A sync separator gives horizontal sync pulses to the Q1 detector. It compares the sync pulses with the pulses of the horizontal oscillator. The H–oscillator is a 6 MHz oscillator from which via a 192: and a 2:divider pulses of 15625 Hz are obtained. The Q1 detector synchronizes the 6 MHz oscillator. The 15625 Hz pulses of the 2:divider synchronize the sawtooth oscillator.
A Q2 detector compares the phase of the sawtooth generator pulses with the line flyback pulses. An output stage supplies at pin 17 drive pulses for the line output stage. A vertical integrator filters out the frame sync pulses and these pulses drive a 625:divider which retrieves 50 Hz pulses from the 192:divider. The sawtooth generator gives a synchronized sawtooth pulse to an amplifier which in its turn drives the frame output stage.
A protection circuit checks whether there is frame deflection, if this is not the case, the level of the burst key pulse is lifted resulting in blanking of the complete picture.

8.2 Input circuit and video switch (see fig. 8–2)

In the sync IC a choice can be made between video of front–end or of scart. This choise is made through the operation via I^2C bus.
After the switch the signal is clamped and goes into two directions. At pin 3 of the IC the video comes out for the chroma section. Internally it goes via a noise inverter to the synch seperator.

8.3 Horizontal sync separator (see fig. 8–3)

The video signal enters on the clipper and when SK 1 is closed on an integrator (R and C2549). This integrator will determine the clipping level of the clipper.

- In sync situation
  The sync pulse coincides with the H–pulse. The coincidence detector switches SK 2 in the "in sync" mode. As a result SK1 is closed during a period that equals 2 sync pulses.
  Consequently, the voltage at pin 27 equals a voltage that lies between the sync peak and the black level (see fig. 8–4). The clipper will allow anything above the clip level to pass. The resultant sync pulses are used to synchronize the H–oscillator. Moreover, the coincidence detector switches on a gating circuit so that the horizontal oscillator can only be synchronized during the sync pulse. In this way the system is not affected by echos and false sync pulses.

- Out of sync situation
  The coincidence detector sees a difference in phase between sync and H–pulse so that SK 2 is switched in the "out of sync" mode. Then SK 1 is driven by a delayed sync pulse. The voltage on the integrator is much higher (see fig. 8–5). As a result the clipper clips much higher so that every pulse that comes through has to be a sync pulse. Furthermore, the gating circuit is switched off so that anything that exceeds the clip level is allowed to pass.

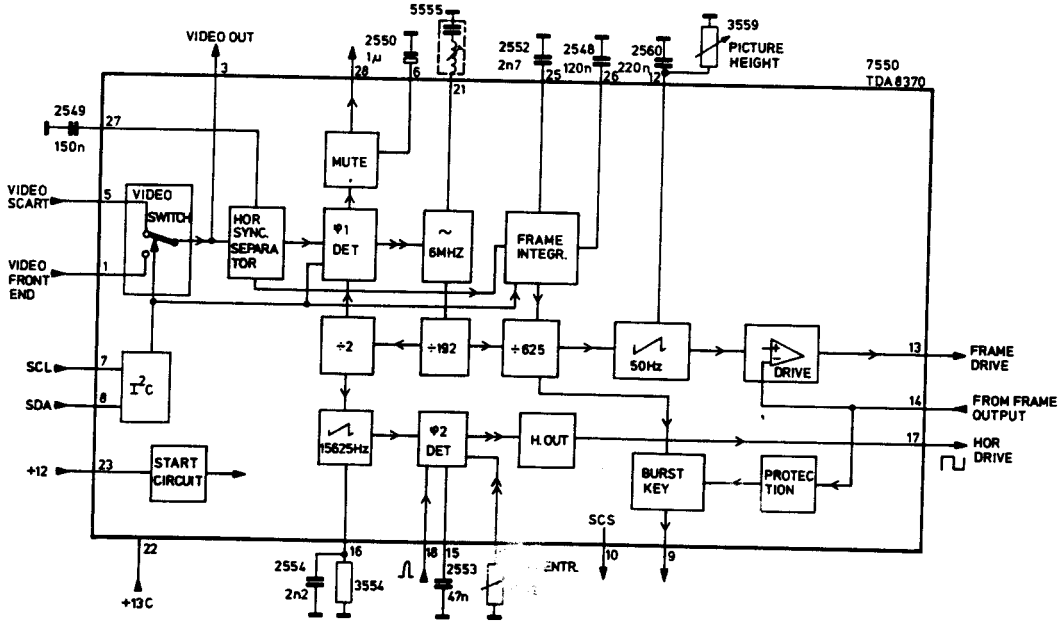


Fig. 8-1

42 214 812

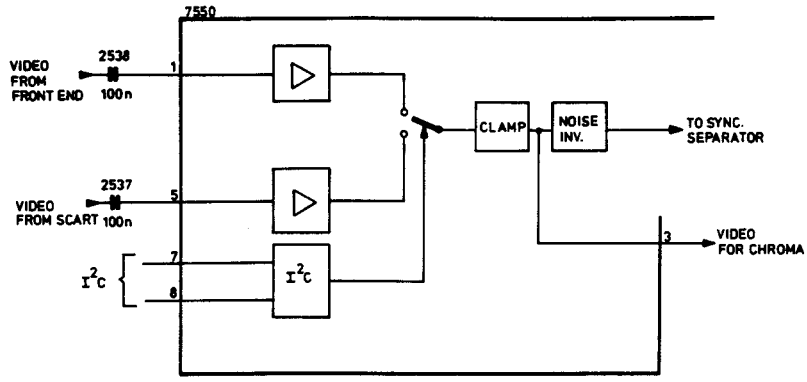


Fig. 8-2 42 221 B12

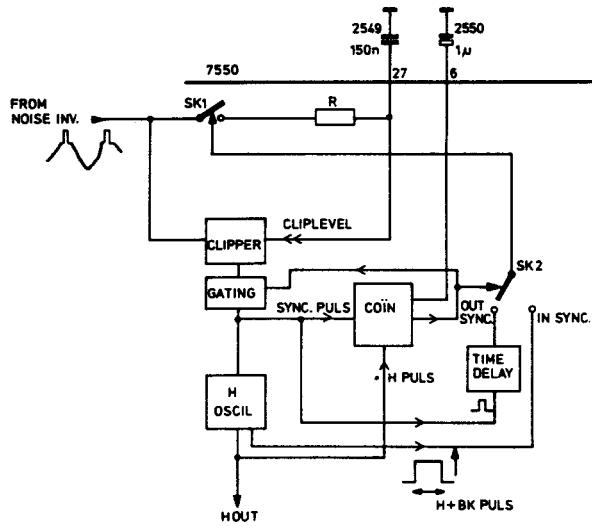


Fig. 8-3 42 222 B12

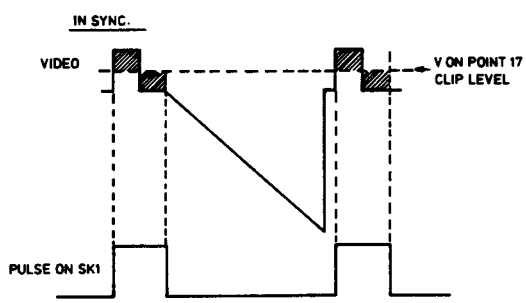


Fig. 8-4 42 197 A12

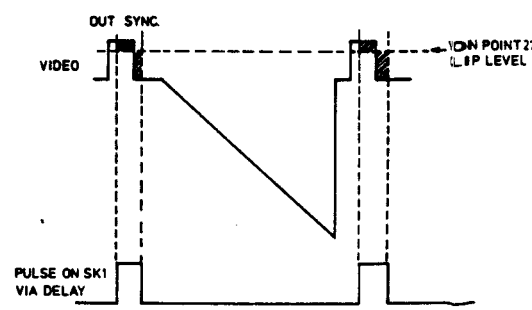


Fig. 8-5 42 198 A12

8.4 Oscillator, detectors Q1 and Q2 and output stage (see fig. 8-6)

The horiz al oscillator is formed by a 6 MHz oscillator. A 192:div gives pulses of 31 250 Hz, these pulses are divide y 625. Thus we obtain 50 Hz sync pulses for the fra e synchronization.
A 2:divider divides the 31 250 Hz pulses so that we obtain pulses of 15 625 Hz.
The Q1 discriminator compares the sync pulses with the 15 625 Hz pulses of the divider. In case of frequency deviations the detector readjusts the 6 MHz oscillator.
The sync pulses of the 2:divider synchronize a 15 625 Hz sawtooth generator.
The Q2 detector compares the phase of the sawtooth generator with a line flyback pulse. In case of phase errors the Q2 detector corrects the output pulse.

8.4.1 Q1 detector (see fig. 8-7)

The Q1 detector receives the H-pulse as input signal. Switch SK 1 is closed during the sync pulse that comes from the separator. C2544, C2545 are charged and discharged by the H-pulse (via two current sources). With good synchronization there is as much as charging as discharging so that the charge of C2544 does not change. With frequency errors C2544 will be charged more or less so that the voltage at pin 24 wil be higher or lower. With this voltage the 6 MHz oscillator is readjusted. In the VCR mode the current sources of the Q1 detector are changed via I^2C bus so that it responds faster.

8.4.2. Sawtooth generator (see fig. 8-8)

The sawtooth generator is formed by a switch with level detector. The level detector closes the switch at approx 4 Volts. As a result C2554 is charged very quickly. At 7 Volts the level detector opens the switch and C2554 discharges across R3554. When a sync pulse arrives, the switch closes immediately.
The 6 MHz oscillator can be adjusted by bringing pin 2 of the sync IC above the 7 Volts. When no signal arrives a circuit itself will bring pin 2 above the 7 Volts so that the oscillator will be running at its nominal frequency (Q1 detector switched off).

8.4.3. Q2 detector (see fig. 8-9)

The Q2 detector consists of 2 current sources. These are driven by the sawtooth pulse. The positive part of the sawtooth pulse opens current source I, the negative part opens current source II.
SK 1 is closed by the line flyback pulse. If the phase of the line flyback pulse and the sawtooth pulse are correct, C2553 is as much charged as discharged. The voltage at pin 15 will not change then. When the phase is not correct, C2553 is charged or discharged more so that the voltage at pin 15 of the IC becomes higher or lower. This voltage will correct the phase of the H-pulse in the horizontal pre amplification stage.

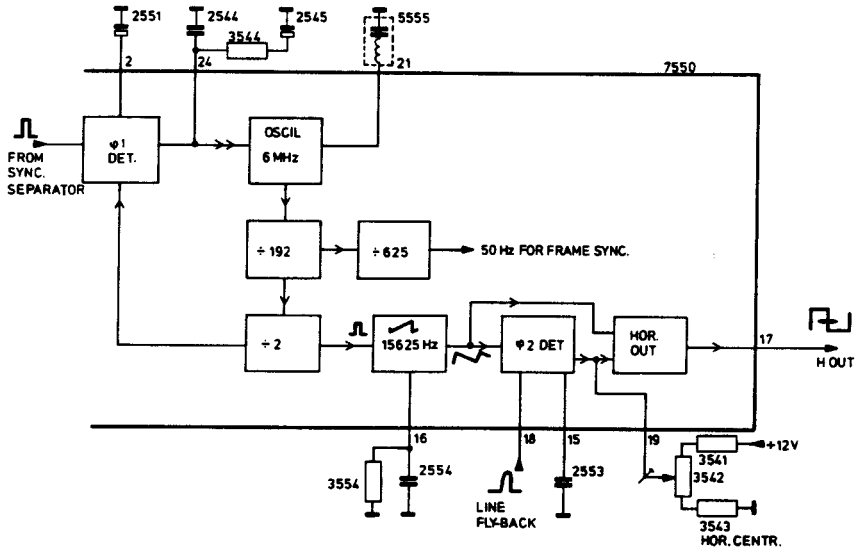


Fig. 8-6 42 217 B12

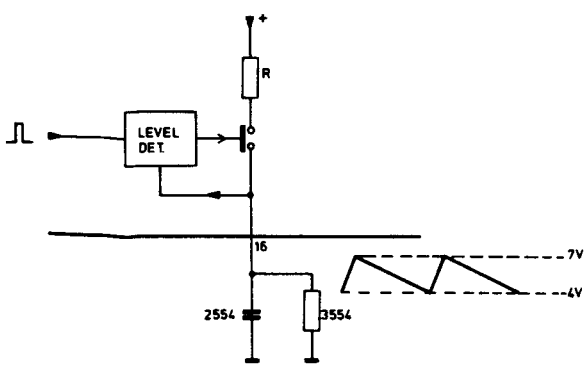


Fig. 8-8 42 208 A12

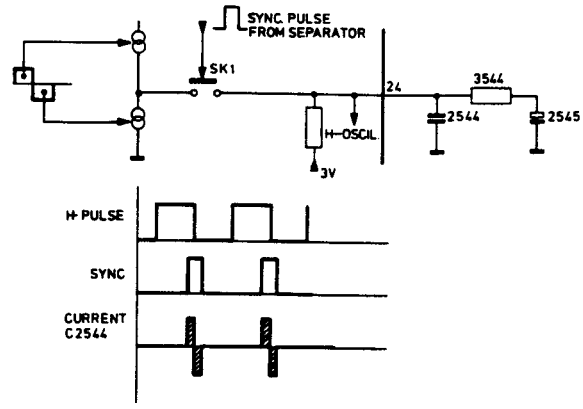


Fig. 8-7 42 218 B12

8.4.4 Horizontal pre amplification stage (see fig. 8–10)

The horizontal pre amplification stage consists of an op–amp. At the + input appears the sawtooth voltage and at the – input the control voltage of the Q2 detector. As output pulse a square wave arises. The positive edge of this square wave may according to the DC voltage of the Q2 detector (phase of H–pulse and line flyback) shift to the left or to the right. At the – input of the op–amp also appears a control voltage. Through variation of this voltage we can let take place the synchronization of the entire frame sooner or later. This is the horizontal centring.

8.4.5. Sync composite sync pulse (S.C.S.)

The sync composite sync pulse is a pulse that is generated by the sync IC at pin 10 (see fig. 8–1). This pulse can be used to synchronize the TXT decoder. In case of noise this signal will still be present so that the TXT picture stays synchronized.

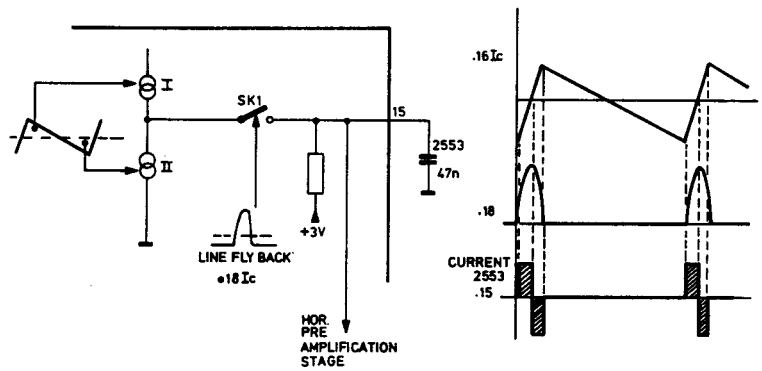


Fig. 8-9

42 219 B12

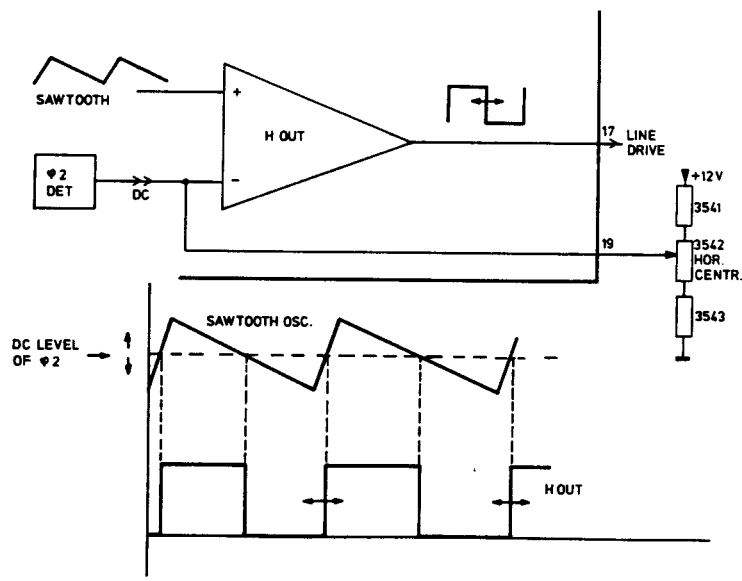


Fig. 8-10

42 220 B12

8.5 Vertical synchronization (see fig. 8–11)

The vertical sync separator consists of an integration network. The resultant sync pulses are fed to two clip circuits. The choise between the two is made by the operation via I²C. In the VCR mode clipper II is switched on. In the normal working clipper I is switched on.
In the VCR mode clipper II drives a pulse shaper that will drive the 625:divider. In the non VCR mode clipper I drives the 625 divider. The sawtooth generator will then drive a driver stage that will drive the frame output stage.

8.5.1 Frame integrator and clippers (see fig. 8–12)

The frame integrator consists of a resistor in the IC and C2552 that has been mounted outside the IC.

- Standard signal.
  In case of a standard video signal SK 1 and SK 2 have been switched in mode I via I²C. As a result clipper I is switched on. The clip level of clipper I is determined by the circuit with R 1 / R 2 / C 1. Since R 1 and R 2 are equal and at one side the peak sync is presented to the circuit and at the other side the black level, the clip level will lie between black– and peak level. The clipper gives frame sync pulses that synchronize the 625 divider. The 50 Hz pulses of the divider are used to drive the vertical sawtooth generator.

- Non standard signal (VCR)
  With VCR the frame and line pulse are made and taped by the video recorder itself. These signals are not identical with the normal sync pulses (duration may differ). That is why in case of VCR a second clipper will be switched on. The operation switches SK 1 and SK 2 are then in mode II. The clip level of clipper 2 is determined by R 3 and R 4. Because of the selection of R 3 and R 4 that clip level lies very high. The sync pulses which the clipper allows to pass are used to drive a pulse shaper. These pulses are of a fixed width and will drive the 625:divider. The result is a more stable frame synchronization.

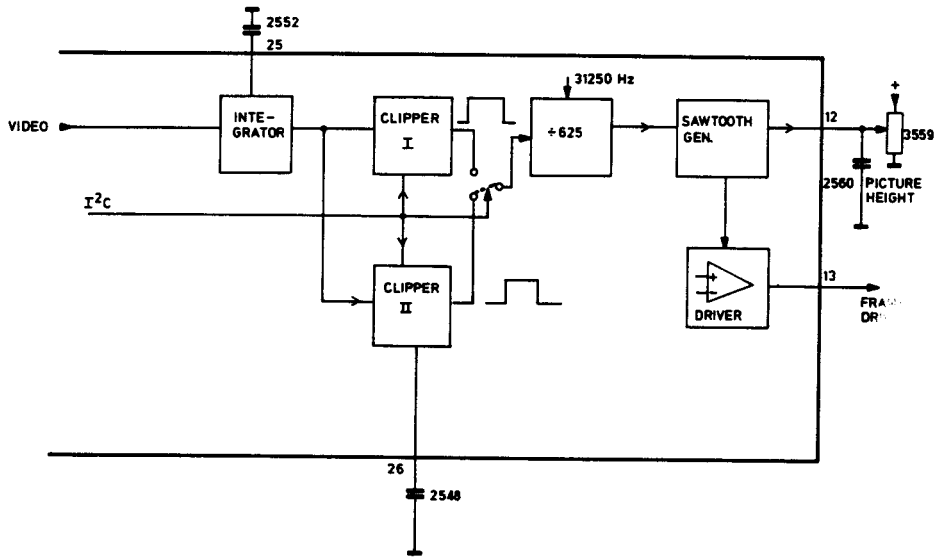


Fig. 8-11

42 215 B12

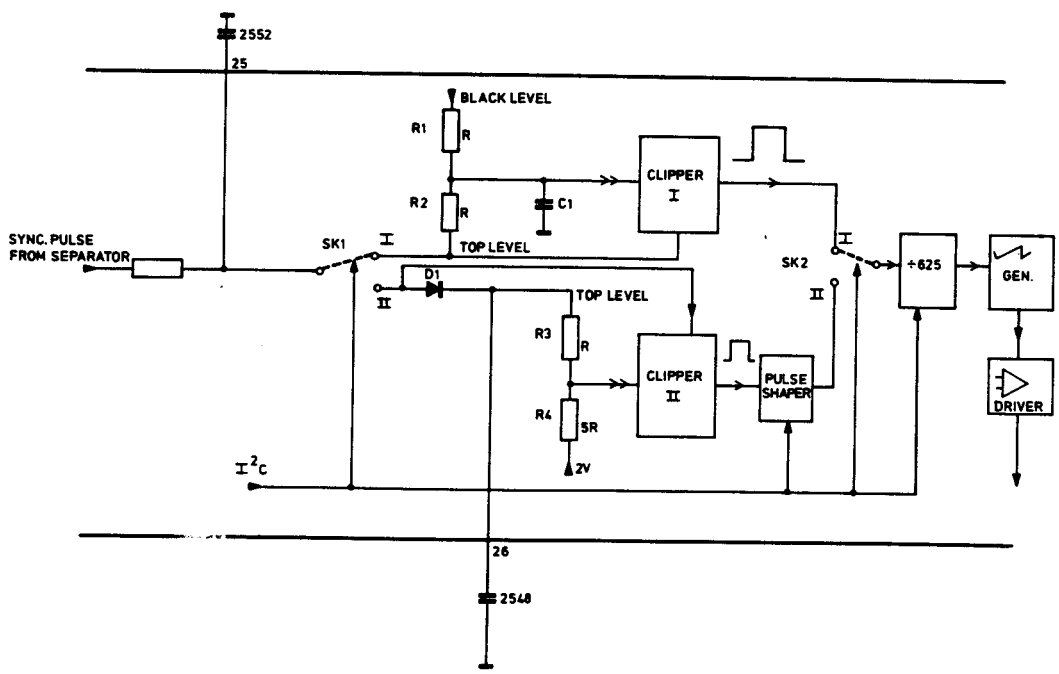


Fig. 8-12

42 216 B12

8.5.2 PAL anti-copy guard.

To prevent copying of video tapes the manufacturers sometimes leave out up to 3 frame sync pulses. In the sync IC a circuit has been provided which makes that when frame pulses have been left out the IC itself will generate them. This generation of frame sync pulses is limited to 3 pulses.

8.5.3 Sawtooth generator (see fig. 8-13)

The sawtooth generator is formed by C2560 that is charged by a resistor network R3558, R3560, R3559. Capacitor C2560 is charged until a sync pulse arrives from the 625 divider. Then switch SK is closed and C2560 is discharged very quickly. At 2 Volts the switch is opened again and charging restarts.
The speed of charging is controlled with R3559 (this is the picture height controller). Internally the sawtooth receives a slight parabola formation which ensures that a linear deflection is obtained.
In case of TXT the frame sawtooth is shifted half a line every 2 frames so that we obtain a non-interlaced picture.

8.5.4. Starting up of sync IC (see fig. 8-1)

When the voltage at pin 23 rises the sawtooth voltage at pin 16 starts to rise. When the sawtooth voltage exceeds 3 Volts the horizontal pre amplification stage can give a pulse at pin 17.
At first the duty cycle of this pulse is very small. It allows the line output stage to give a voltage of 12 Volts at pin 22. When the voltage at pin 22 exceeds 9,5 Volts the IC will increase the duty cycle and proceed to a normal operating mode.

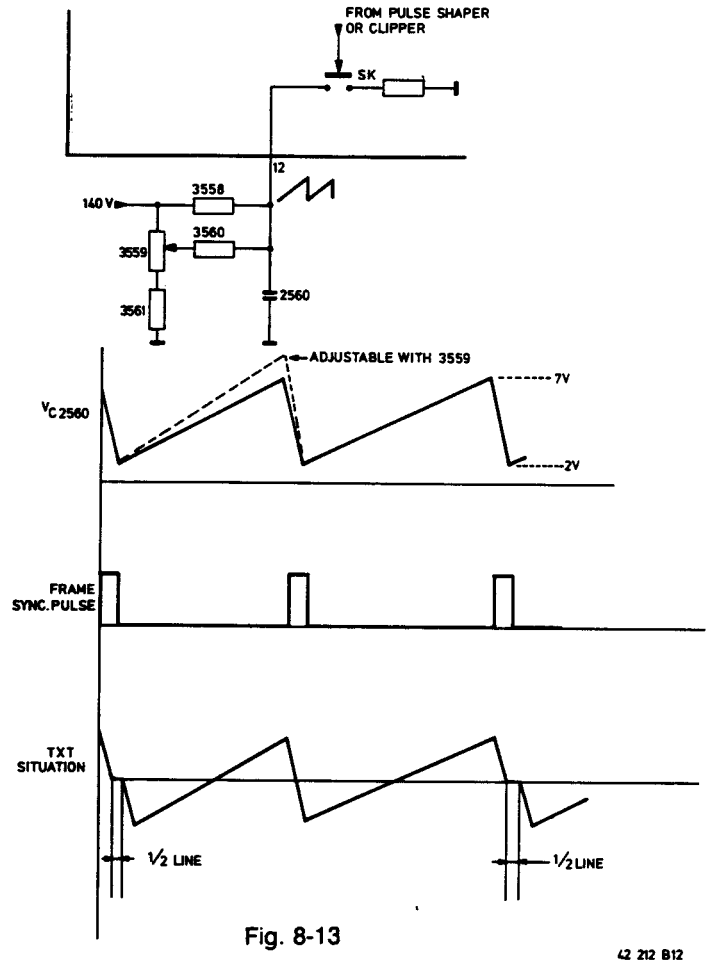


Fig. 8-13

42 212 B12

9. FRAME OUTPUT AMPLIFIER (see fig. 9-1)

The frame output stage in IC7570 is driven by the driver stage in sync IC7550.
The amplitude and the shape of the sawtooth on the output is determined by the feedback circuit C2564, R3565, R3575 and C2575.
In the IC is a flyback generator which arranges that, at the moment of the vertical flyback pulse, the supply voltage of the output amplifier is temporarily increased by the voltage that has been built up across C2571 during the scan time.
This temporary increase in voltage is needed to obtain the desired flyback time. In this way the supply voltage can stay low, causing the dissipation to be as low as possible.
The output amplifier contains a protection circuit which keeps the dissipation within well-defined limits and a thermal protection which switches the circuit off when the temperature of the IC exceeds 175°C.

The IC also contains a supply voltage stabilizer which keeps the voltage constant despite the high load current.
The shape of the output voltage of the output amplifier is now such that a sawtooth current will flow through the vertical deflection coil.
The vertical position of the picture can be selected with SK4.
The resistor that has been applied across the deflection coil and C2572 serve to damp the line-frequent voltages in the vertical deflection coil, so that no line-interlace faults occur.

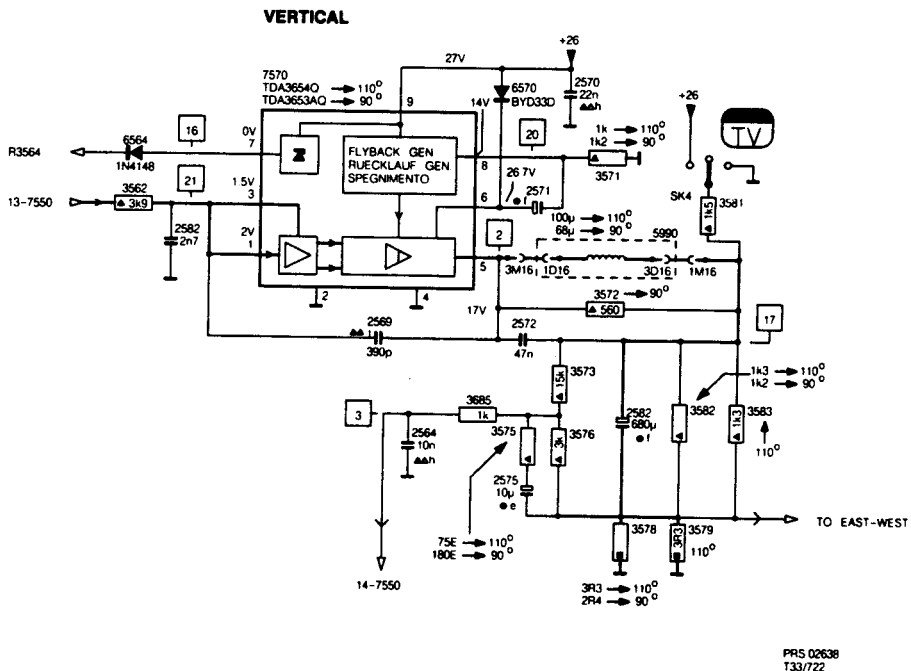


Fig. 9-1

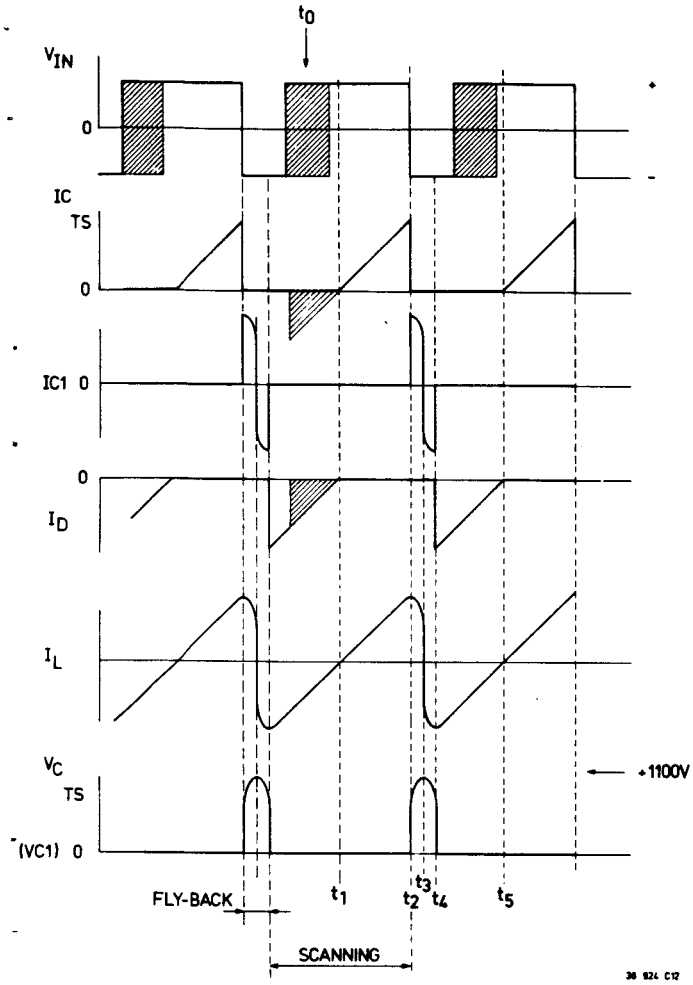


Fig. 10-3

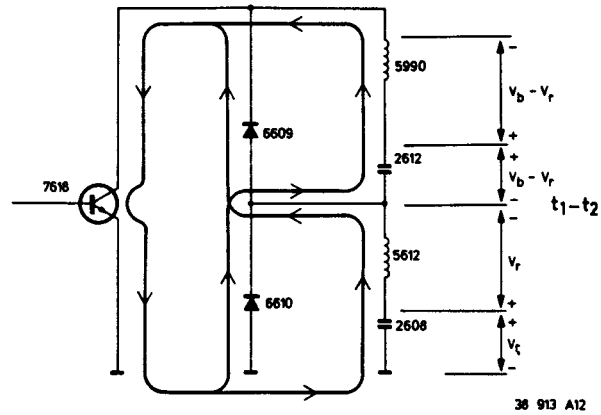


Fig. 10-6

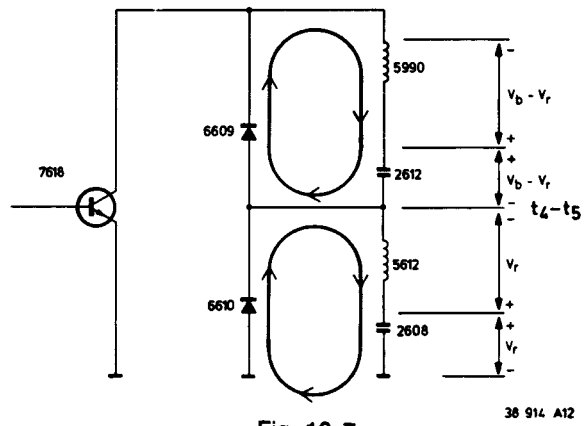


Fig. 10-7

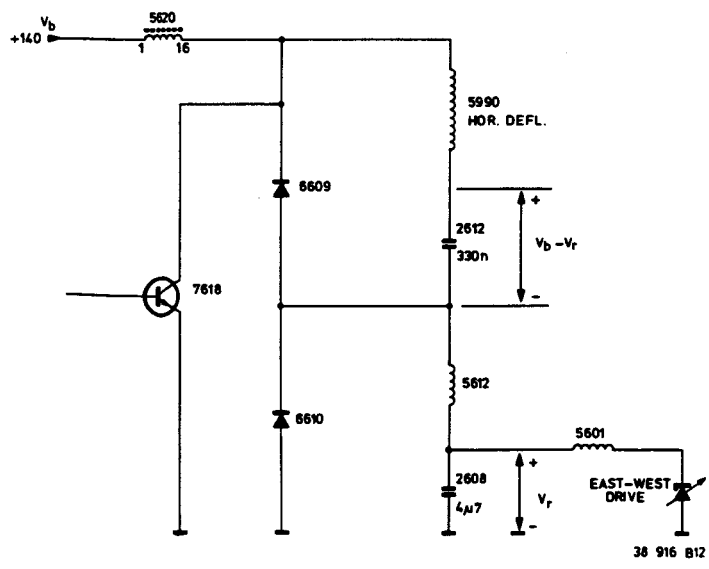


Fig. 10-5

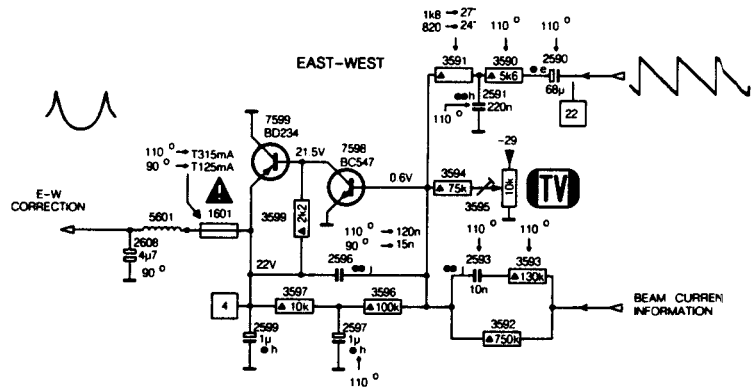


Fig. 10-4

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T33/72

10. HORIZONTAL OUTPUT STAGE

10.1 Horizontal deflection circuit

The complete circuit is given in Fig. 10-1 and Fig. 10-2 is a simplified diagram.
Via the primary of line output transformer T5620 and deflection coil L, capacitor C2 is charged to 140 V (see Fig. 10-2). This charge remains virtually constant because C2 has a large value. The drive for transistor TS comes from sync IC7550.
During t_1-t_2 the drive voltage is positive (see Fig. 10-3) and transistor TS is saturated, and its collector voltage zero. As a result L is parallel to C2 so that a constant voltage of 140 V appears across this coil. Now a sawtooth current will flow through L and TS.
At t_2 the drive voltage becomes negative and TS switches off. The current which flowed through L, flows on through C1, thus bringing energy from L to C1. The current through L drops and the voltage across C1 rises sinusoidally.
In time t_3 all energy from L has been transferred to C1 and energy recovery starts during t_3t_4. Now C1 feeds current back to L so that the voltage across C1 drops and the current through L is sinusoidal. If all energy from C1 were now again transferred to L the voltage across C1 would want to become negative. However, diode D starts conducting at t_4 causing L to be reconnected to C2. The voltage across L once again is 140 V which results in the same $\Delta I/\Delta t$ as during t_1.
The moment the current wants to change direction TS takes over the current because it received prior to this point in time a positive control voltage during time t_0. Time t_0 should always come before t_1 (in hatched section of Fig. 10-3) to ensure that TS is conducting in time.

In reality L is the series circuit of the horzontal deflection coil and S5612, C1 is C2617 and C2 is the series circuit of C2612 and C2608 (see Fig. 10-1). L and C2 have been split in two to enable east-west correction. For, if the horzontal deflection current is always equally great, a picture with horizontal pin-cushion is formed. To eliminate this fault, the horizontal deflection current should be modulated by the east-west generator.

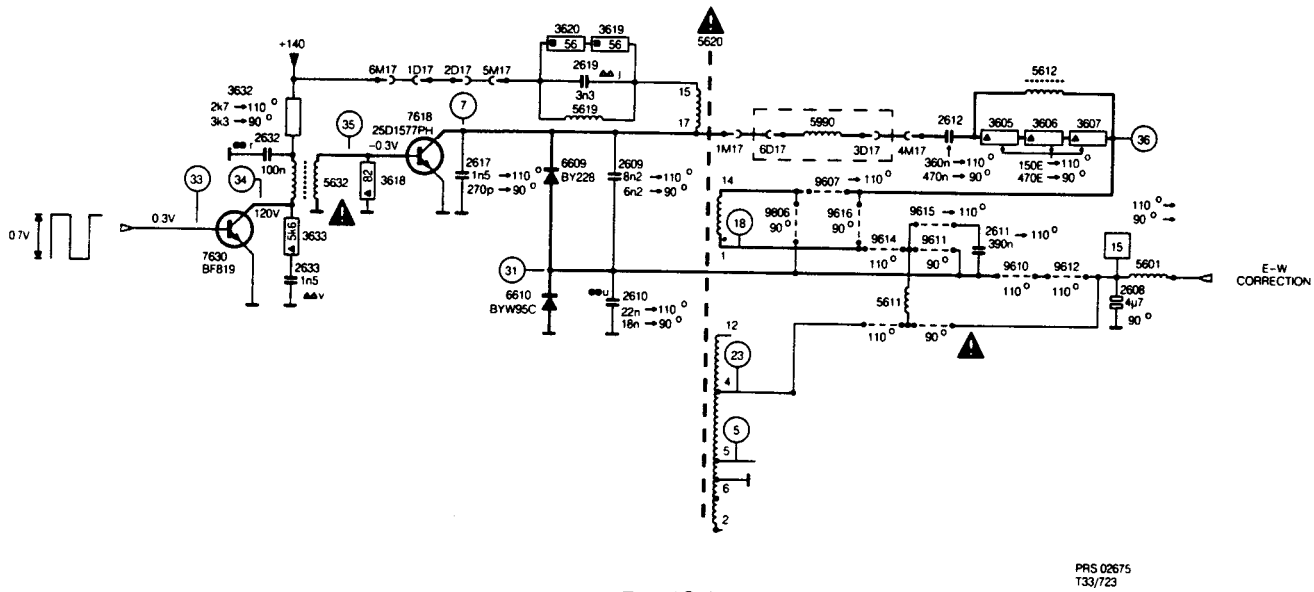

Fig. 10-1

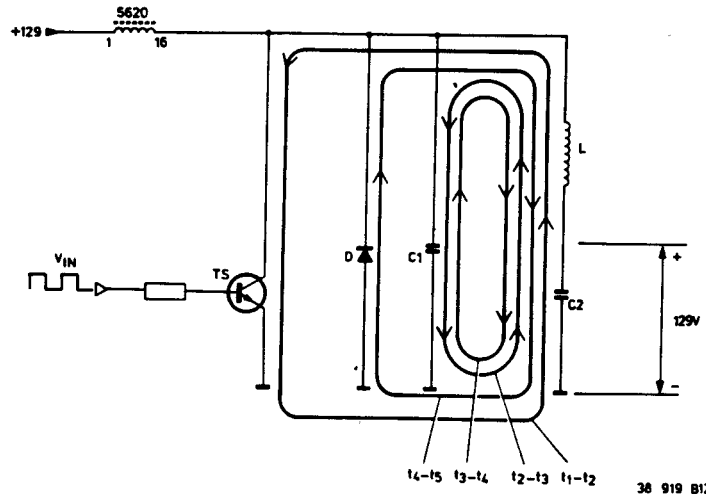

Fig. 10-2

10.2 East-west correction

The east-west generator is shown in Fig. 10-4 and the modulation circuit in Fig. 10-5.
The picture width is determined by the scan voltage across S5990 during t_1-t_2 and t_4-t_5. If this voltage is changed, the picture width is controlled also. The scan voltage always equals Vb-Vr.
If S5601 is not present Vb will be distributed between C2612 (Vb-Vr) and C2608 (Vr) dependent on the self-inductances of S5990 and S5612, as well as on capacitances C2612 and C2608.
Vr becomes approx. 30 V and the voltage of C2612 (Vb-Vr) will then be 110 V (30 + 110 = 140 V).
This implies that during t_1-t_2 and t_4-t_5 a voltage of 110 V is present across S5990 and a voltage of 30 V across S5612. In this case the picture width is always too small. By discharging C2608 via S5601 by means of the east-west control (represented by an adjustable zener diode), Vr can be made to drop and Vb-Vr can be made to rise, which yields a picture width increase.
So, the picture width increases when Vr decreases.
S5601 serves to block the line frequency current to the east-west generator. Fig. 10-6 gives the currents during t_1-t_2 and Fig. 10-7 those during t_4-t_5.

The required parabolic correction is obtained because via C2590-R3590-R3591 a sawtooth voltage is fed to integrator TS7599-TS7598-C2596 where it is converted into a parabolic voltage. As a result Vr will increase at top and bottom of the picture thus reducing the picture width.
In the centre of the picture Vr decreases thus increasing the picture width.

The east-west corrections perform the following three functions:
- It determines the average picture width (average value of Vr).
- It adapts the value of Vr to the average beam current. If the beam current rises Vr should rise to, thus avoiding horizontal blooming.
- It modulates Vr with a frame frequency parabolic voltage, in order to eliminate east-west pin-cushion distortion.

By means of the circuit with TS7599-TS7598 (Fig. 10-4) C2608 is discharged. C2608 cannot be charged by this circuit because the current through TS7599 can flow in one direction only.
The DC setting (picture width determining) is obtained by R3597 and R3596 while C2597 ensures that there is no AC negative feedback.
With R3595 the picture width is adjusted. Via R3592, C2593, R3593 the picture width is corrected for beam current variations.

10.3 High voltage (Fig. 10-8)

The high voltage is obtained by rectifying the AC voltages across the high voltage winding and by adding them according to the diode-split method. The pulse voltage across winding a-b is rectified by D1, as a result of which the so-called intermediate layer capacitance C1 will be charged to a DC voltage equalling the peak voltage across winding a-b.
The pulse voltage across winding c-d is rectified by means of D2, resulting in a DC voltage across C2 equalling the peak voltage across winding c-d. The pulse voltage across winding e-f is rectified by D3 as a result of which C3 is charged to the peak voltage across winding e-f. In this way a DC voltage of approx 25 kV is formed.

The DC voltage formed after rectification of the pulses across winding a-b (approx 6,25 kV) is used for focusing with U1474. With R3472 the Vg2 voltage at pin 10 of the picture tube is adjusted.

The beam current information present across R3496 is passed on to:
a. The east-west generator to compensate for picture-width variations.
b. The contrast voltage to reduce it when the beam current becomes too great.

In the high voltage cable two resistors have been incorporated with the following purpose:
a. Preventing a complete short-circuit of the line output transformer in case of flashover in the picture tube.
b. Preventing radiation of the line frequency or its harmonics, which would cause interference at LW and MW for radio receivers.

The heater voltage of the picture tube is supplied by winding 8-10 of T5620.

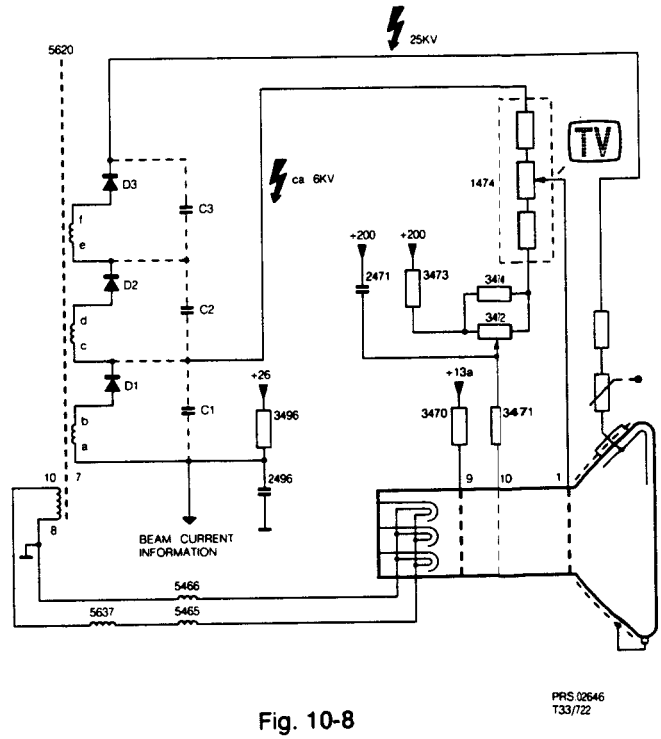

Fig. 10-8

10.4 Derived supply voltages

These voltages are obtained after rectification of the line pulses by means of the circuit according to Fig. 10-9.

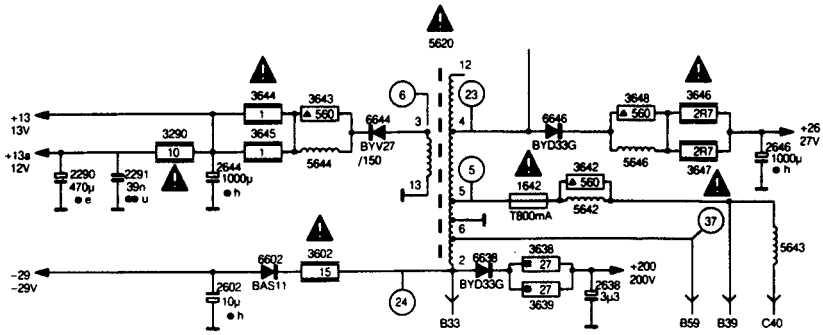

Fig. 10-9

PRS 02673
T33/723

11. PICTURE TUBE CORRECTIONS

In sets having picture sizes 21", 24" and 27", a picture tube of the flat square type has been applied. This picture tube also forms an integral system with the glued delflection unit so that no picture corrections are required.

13.1 Introduction

13.1.1 Block diagram (see Fig. 13-1)

The FST-6 system is a digital control system based on frequency synthesized tuning.
The system consists of microprocessor IC7830 which drives CITAC IC7900 and the memories IC7925 and IC7926. (CITAC is the abbreviation for Computer Interface for Tuning and Analogue Control).
Communication between the microprocessor and the various blocks takes place by means of the inter-IC bus in short I²C bus. This bus consists of a serial data line (SDA) and a serial clock line (SCL).
For more information on the I²C system reference is made to appendix 1.
The commands from the control panel (keyboard) and the remote control (remote receiver) are processed by the microprocessor and via the I²C bus in digital form fed to the CITAC IC7900. This CITAC IC converts all digital signals into various control voltages (see Fig. 13-1). If, for instance, a command is given for selection of a certain program number, CITAC IC7900 will deliver a tuning voltage (V tune) to which the channel selector will tune. The "prescaler" and "AFC interface" blocks serve to ensure a good tuning procedure and to keep the tuning voltage constant. See chapter 13.3 for more details on the tuning procedure.
Superfluous memories IC7925 and IC7926 are used to store various data. Such as the selected channel numbers and the set values of volume, brightness, etc.
If the set is switched off, the memories are supplied with voltage by battery 1925.

Via the reset interface microprocessor IC7830 detects a power on reset when the set is switched on. Via the I²C bus information is also sent to the teletext circuit or the viewdata circuit if they are available.
The system receives its supply voltages from the main supply of the set.
In the stand-by mode the main supply also delivers the +5 V voltage.

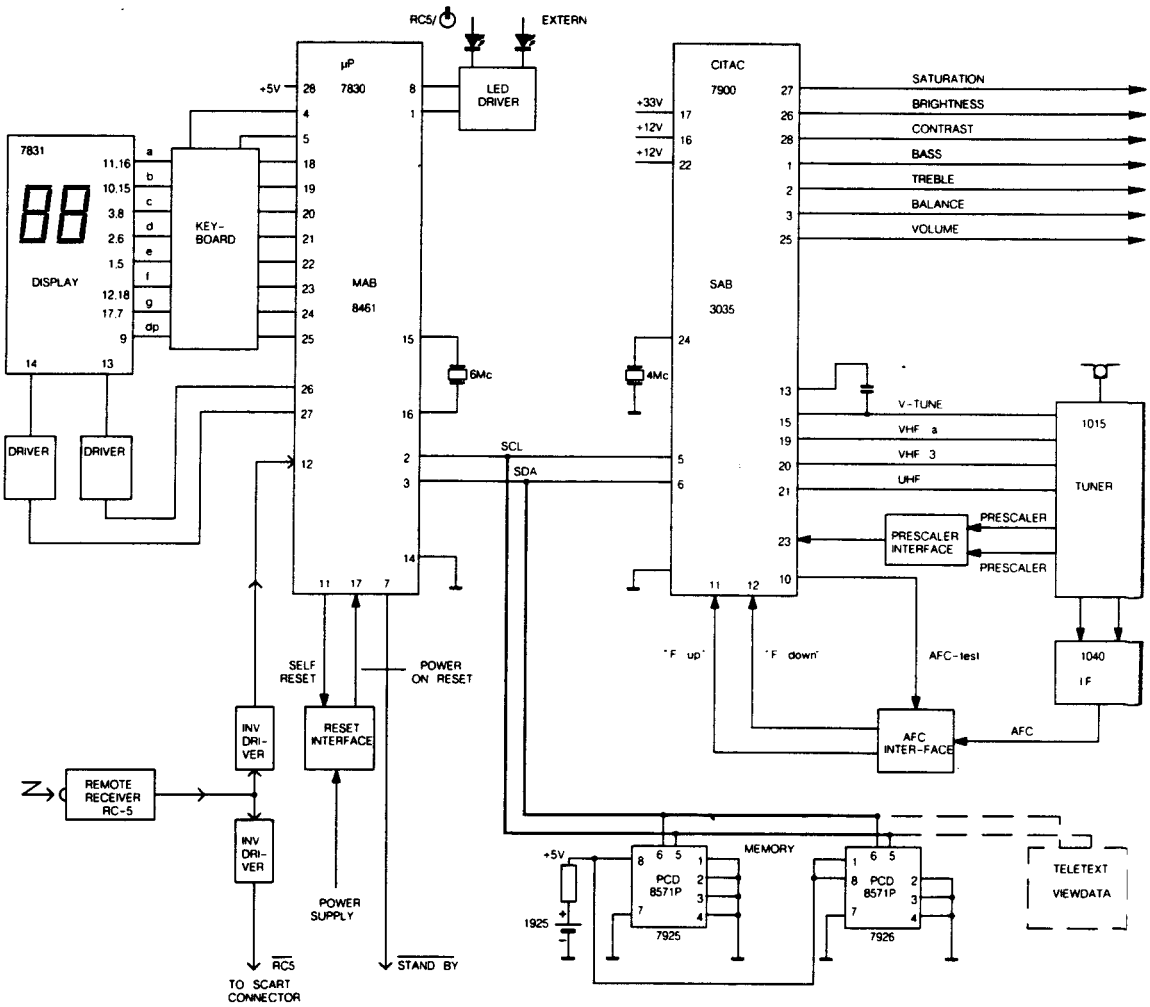

Fig. 13-1

PRS 02629
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T33/722

13.1.2 Control possibilities

The system offers the following possibilities:

a. Direct program selection
   Here a distinction can be made between
   - one-digit mode: programs 0 to 9 by keying one digit
   - two-digit mode: programs 00 to 49, for the 50-fold system, by keying two digits.
   - the possibility to increase or decrease the program number step by step (step +, step –).

b. Direct channel selection
   Here always two digits should be keyed. It is also possible to increase or decrease resp. the channel number by means of the step + and step – keys.

c. Automatic transmitter searching by means of the so-called "search tuning". An automatic searching which starts by depressing key(▷▷|).

d. Other possibilities
   Here we can distinguish:
   - channel/program mode selection via the (C/P) key.
   - store open (◇)and store execute (◇) functions to record the selected data. Via key (◇)and key (◇).
   - sound on/off via key (🔇).
   - control and storage of a number of analogue functions, such as volume (◿), brightness (☼), saturation (◕), contrast (◐), bass (♪), treble (♪) and balance◺.
     Storage is possible via the store execute key (◇) and reading of the data via the "personal preference"/PP key (▸▢◂).
     selection of the stand-by mode via the stand-by key (⏻).
     selection of an external video source entering via SCART by pushing key ◧▸.

13.2 Control

13.2.1 Remote control

Transmitter U1850 (see Fig. 13-2) emits infrared light to receiver U1840. The transmitter delivers these infrared light pulses according to the RC5 code (see Fig. 13-3). The code is repeatedly transmitted when the key remains depressed. Via transistor TS7856 that acts as inverter the RC5 signal arrives at pin 12 of microprocessor IC7830.
Via transistor TS7853 the RC5 signal is fed to pin 8 of the euro connector (SCART) for possible remote control of external equipment.
During each RC5 command the microprocessor drives via pin 8 and transistor TS7845 the RC5 LED D6845. The flashing of the LED shows that the RC5 command is received.
The serial RC5 data are decoded and processed by the program of microprocessor IC7830.

13.2.2 Local keyboard and display

The local keyboard presents the possibility of connecting 16 keys ordened in a matrix of 2 columns and 8 rows. The eight lines used by microprocessor IC7830 to drive the display are at the same time the 8 rows of the keyboard matrix and are used for a certain period of time to read data from the keyboard in microprocessor IC7830
By means of pins 26 and 27 of microprocessor IC7830 it is indicated if the tens or the units of the program numbers are presented (see Fig 13-2).

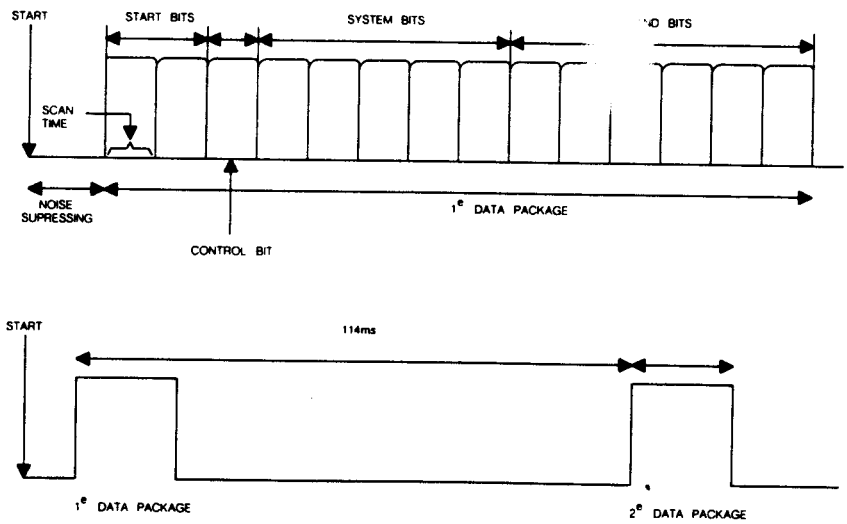
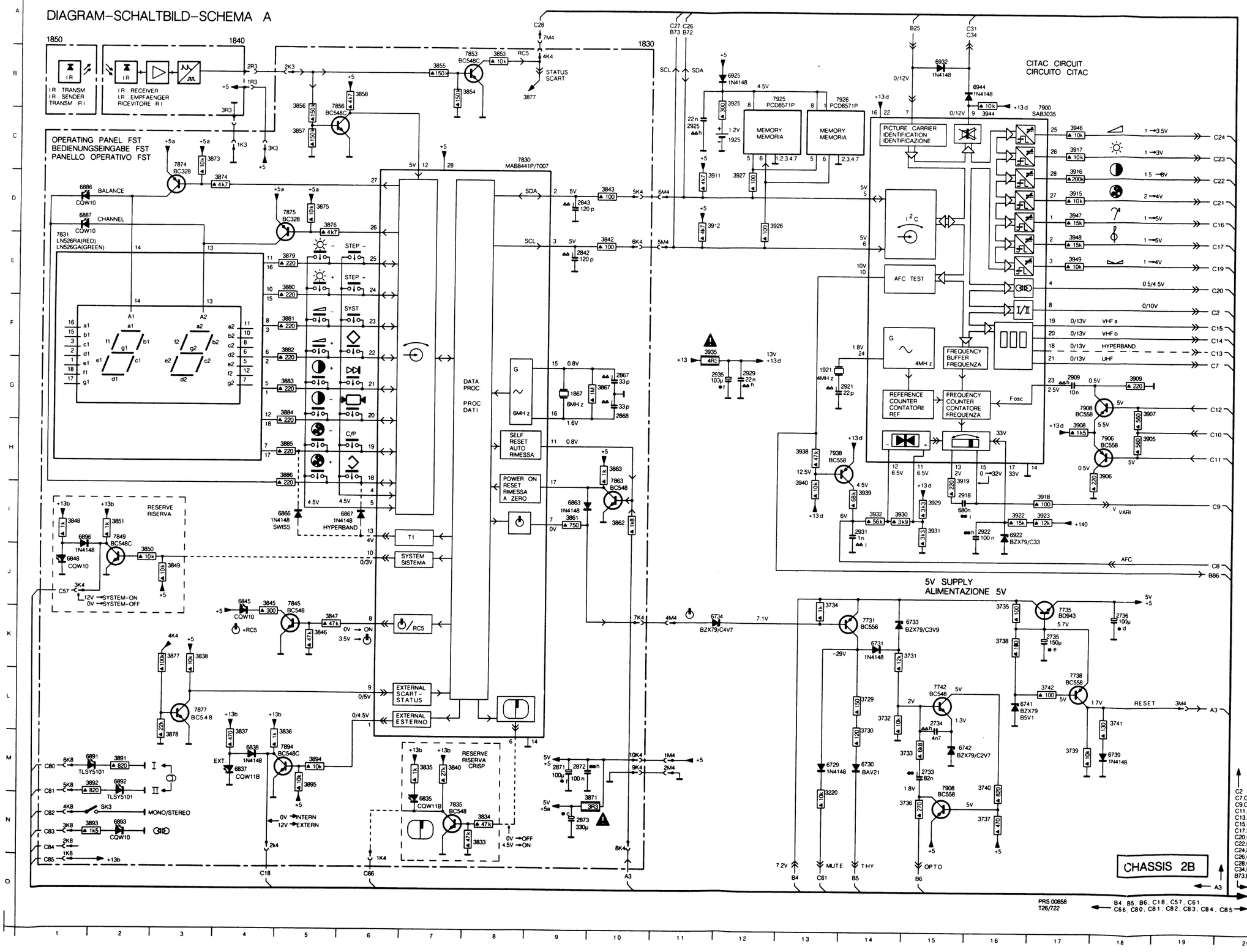


Fig. 13-3

MDA 00180
T32/727

DIAGRAM–SCHALTBILD–SCHEMA A



1840	A 4	7830	C 8
1850	A 1	7831	E 1
1867	G 9	7835	N 7
1921	G13	7845	J 5
1925	C12	7849	I 2
2733	M15	7853	B 7
2734	L15	7856	B 5
2735	K17	7863	H10
2736	K18	7874	C 3
2842	E 9	7875	D 5
2843	D 9	7877	L 3
2867	G10	7894	M 5
2868	G10	7900	B17
2871	M 9	7906	H18
2872	M 9	7908	G17
2873	N 9	7908	M15
2909	G17	7925	B12
2918	I 15	7926	B13
2921	G14	7938	H13
2922	I 16		
2925	C11		
2929	G12		
2931	I 14		
2935	G12		
3220	M13		
3729	L14		
3730	L14		
3731	K15		
3732	L14		
3733	M15		
3734	J13		
3735	J16		
3736	N15		
3737	N16		
3738	K16		
3739	M17		
3740	M16		
3741	L18		
3742	L17		
3833	N 8		
3834	N 8		
3835	M 7		
3836	M 5		
3837	M 4		
3838	M 3		
3840	M 7		
3842	E10		
3843	D10		
3845	J 4		
3846	K 5		
3847	K 5		
3848	I 1		
3849	J 3		
3850	J 2		
3851	I 2		
3853	B 8		
3854	B 8		
3855	B 7		
3856	B 5		
3857	C 5		
3858	B 6		
3861	I 9		
3862	I 10		
3863	H10		
3867	G10		
3871	N10		
3873	C 3		
3874	D 4		
3875	D 5		
3876	D 5		
3877	K 3		
3878	M 3		
3879	E 5		
3880	E 5		
3881	F 5		
3882	F 5		
3883	G 5		
3884	G 5		
3885	H 5		
3886	H 5		
3891	M 2		
3892	M 2		
3893	N 2		
3894	M 5		
3895	M 5		
3905	H18		
3906	H18		
3907	G18		
3908	G17		
3909	G18		
3911	D11		
3912	D11		
3915	D17		
3916	C17		
3917	C17		
3918	I 17		
3919	H15		
3922	I 16		
3923	I 17		
3925	B12		
3926	D12		
3927	D12		
3929	I 15		
3930	I 14		
3931	I 15		
3932	I 14		
3935	F 11		
3938	H13		
3939	I 14		
3940	H13		
3944	B16		
3946	C17		
3947	D17		
3948	D17		
3949	E17		
6729	M13		
6730	M14		
6731	K14		
6733	K15		
6734	K12		
6739	M18		
6741	L17		
6742	M16		
6835	N 7		
6837	M 4		
6838	M 4		
6845	J 4		
6848	J 1		
6863	I 9		
6866	I 5		
6867	I 6		
6886	D 1		
6887	D 1		
6891	M 2		
6892	M 2		
6893	N 2		
6896	I 1		
6922	I 16		
6925	B12		
6932	B15		
6944	B16		
7731	K14		
7735	J17		
7738	L17		
7742	L15		

Fig. 13-2

At point of time t_1 (see Fig. 13-4) pin 26 is "high and pin 27 "low", via 8 lines the data for the tens are presented to the display.
At point of time t_2 pin 26 is "low" and pin 27 is "high", now the data for the units are presented. The total program number on the display thus appears at a frequency of about 100 Hz; built of 2 × 4,96 = 9,92 ms lasting the cycle from t_0-t_2 and from t_2-t_4 (see Fig. 13-4).
Within this cycle, from t_0-t_1 and t_2-t_3, upon the transition from units to tens and vice versa, both display segments are briefly switched off by rendering pin 26 and pin 27 of microprocessor IC7830 both high. Now the eight lines will be free to transfer data from the local keyboard to microprocessor IC7830.
Next microprocessor IC7830 renders pins 18 to 25 one by one low for approx 55 µs.
Via the columns of the keyboard matrix that have been connected to pins 4 and 5 of microprocessor IC7830 it is being detected which keys are depressed.
The total scanning time for the keyboard will now be approx 8 × 4,96 = 39,68 ms.

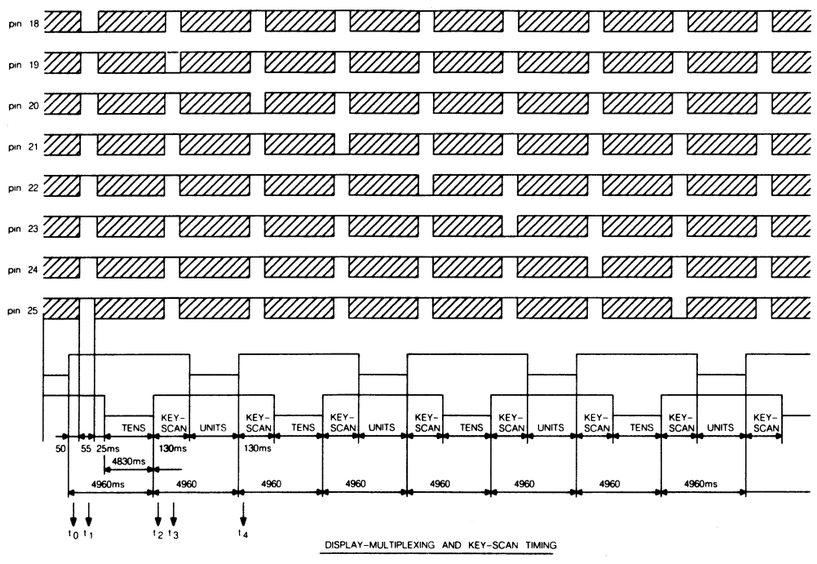


Fig. 13-4

MDA 00186
T33/728

13.3 Tuning procedure

The tuning to a transmitter is based on frequency synthesis (FST) in combination with an automatic frequency control (AFC). The tuning to a certain frequency and the check for the tuning to that frequency is performed by a digital loop and an AFC loop that automatically readjust the frequency.
In the digital loop (see Fig. 13-5) CITAC IC7900 compares a frequency generated by microprocessor IC7830, which is in 15-bit digital form via the I²C bus transmitted to CITAC IC7900, with a frequency that is via a frequency divider coming from channel selection 1015. A tuning voltage Vtuning is derived from it. This tuning voltage readjusts channel selector 1015 so that a new local frequency is returned to CITAC IC7900.
This process is continued until the difference between the local frequency and the frequency generated by microprocessor IC7830 becomes less than 150 kHz. Then the system has been locked in digitally. The digitized tuning frequency has an accuracy of 50 kHz.

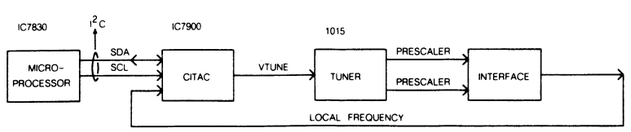


Fig. 13-5

PRS 00706
DRA CS2
T02/727

The frequency generated by microprocessor IC7830 is derived from the table in Fig. 13-8 by the program of microprocessor IC7830. Next the AFC loop becomes operative because the AFC is switched on by CITAC IC7900 (see Fig. 13-6).

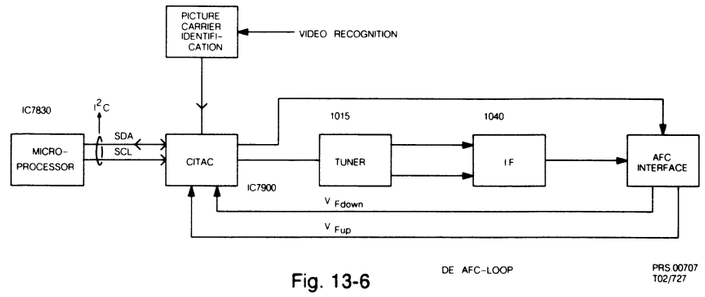


Fig. 13-6

The following situations may occur now:
a. If within approx 500 ms a carrier is identified in a retaining zone of +/– 750 kHz relative to the nominal picture carrier, the AFC will adjust the frequency deviation back to approx 10 kHz.
This is followed by an AFC zero-axis crossing test for about 500 ms.
The first 250 ms an interference signal is applied to the AFC input of CITAC IC7900, next the AFC is tested without interference signal for about 250 ms (see Fig. 13-2).
If a stable tuning situation has been obtained, microprocessor IC7830 wil proceed and establishes, again via CITAC IC7900, if video identification is present.
If there is video identification, the system will be tuned to a picture carrier so that the tuning procedure has been completed.
If there is no video identification present, apparently the carrier to which the system is tuned is no picture carrier and the AFC loop adjusts the frequency outside the AFC retaining zone. Then tuning will be continued with "micro search".

b. If no carrier is identified within 500 ms, the AFC adjusts the frequency immediately outside the AFC retaining zone and next tuning is continued with "micro search". "Micro search" is a search procedure laid down in the program of microprocessor IC7830.

The micro search procedure works as follows:
The selected channel has for instance frequency FB. In the first instance the digital loop described above will want to tune to the nominal frequency (block B4 in Fig. 13-7); because within this B4 block no frequency is found, a range of 7 MHz (VHF) or 8 MHz (UHF) will be searched in steps of 1 MHz according to the cycle below, until the transmitter has been found.
B4, B5, B6, B7, B1, B2, B3 for VHF
B4, B5, B6, B7, B8, B1, B2, B3 for UHF
If a transmitter is found, it will deviate from the nominal frequency (the so-called offset frequency). This offset frequency is stored in the program memory (see chapter 13.5).

As soon as the "search tuning" command is given via keying of key (▷▷|) the system goes from for instance FB to FC, etc. (see Fig. 13-7) in steps of 1 MHz until tuning to a TV transmitter takes place.
If, however, a "search tuning" command is given the moment an attempt is being made to tune to e.g. block B6, the cycle will be as follows for VHF:
B6, B7, B1, B2, B3, C1, C2, C3, C4, C5, C6, C7, D1 ...etc. for UHF
B6, B7, B8, B1, B2, B3, C1, C2, C3, C4, .. etc.
Band selection of the channel selector is the responsibility of CITAC IC7900. CITAC IC7900 makes a choice between UHF and VHFa or VHFb via pin 21, pin 19 or pin 20 of this IC resp. if the related command is given by microprocessor IC7830.
The names FA, FB and FC used are some frequencies from the table in Fig. 13-8.

13.4 Analogue controls

The control voltages for operation of the analogue functions are supplied by 6-bit digital analogue converters situated in CITAC IC7900.
As a result 64 discrete control voltage levels per output are available.
The functions to be controlled are (see Fig. 13-2):

– Volume	pin 25
– Brightness	pin 26
– Saturation	pin 27
– Contrast	pin 28
– Bass	pin 1
– Treble	pin 2
– Balance	pin 3

Moreover, the following switching functions exist:

– Stereo on/off	pin 4
– Language I/II	pin 8

The time to adjust from minimum to maximum is about 7s.
For the contrast function where only 32 discrete voltage levels are required the time to adjust from minimum to maximum is about 3,5 s.
The volume is set to minimum (mute) as long as there is no video recognition.
It is possible to store the values of the set analogue functions in the memory as personal preference values. Via the store execute key (◇).

channel nr.		picture-carrier mhz	flo mhz	band
00		455.25	494.15	uhf
01		463.25	502.15	uhf
02	e2	48.25	87.15	vhf 1
03	e3	55.25	94.15	vhf 1
04	e4	62.25	101.15	vhf 1
05	e5	175.25	214.15	vhf 3
06	e6	182.25	221.15	vhf 3
07	e7	189.25	228.15	vhf 3
08	e8	196.25	235.15	vhf 3
09	e9	203.25	242.15	vhf 3
10	e10	210.25	249.15	vhf 3
11	e11	217.25	256.15	vhf 3
12	e12	224.25	263.15	vhf 3
13	a	53.75	92.65	vhf 1
14	b	62.25	101.15	vhf 1
15	c	82.25	121.15	vhf 1
16	d	175.25	214.15	vhf 3
17	e	183.75	222.65	vhf 3
18	f	192.25	231.15	vhf 3
19	g	201.25	240.15	vhf 3
20	h	210.25	249.15	vhf 3
21	e21	471.25	510.15	uhf
22	e22	479.25	518.15	uhf
23	e23	487.25	526.15	uhf
24	e24	495.25	534.15	uhf
25	e25	503.25	542.15	uhf
26	e26	511.25	550.15	uhf
27	e27	519.25	558.15	uhf
28	e28	527.25	566.15	uhf
29	e29	535.25	574.15	uhf
30	e30	543.25	582.15	uhf
31	e31	551.25	590.15	uhf
32	e32	559.25	598.15	uhf
33	e33	567.25	606.15	uhf
34	e34	575.25	614.15	uhf
35	e35	583.25	622.15	uhf
36	e36	591.25	630.15	uhf
37	e37	599.25	638.15	uhf
38	e38	607.25	646.15	uhf
39	e39	615.25	654.15	uhf
40	e40	623.25	662.15	uhf
41	e41	631.25	670.15	uhf
42	e42	639.25	678.15	uhf
43	e43	647.25	686.15	uhf
44	e44	655.25	694.15	uhf
45	e45	663.25	702.15	uhf
46	e46	671.25	710.15	uhf
47	e47	679.25	718.15	uhf
48	e48	687.25	726.15	uhf
49	e49	695.25	734.15	uhf

channel nr.		picture-carrier mhz	flo mhz	band
50	e50	703.25	742.15	uhf
51	e51	711.25	750.15	uhf
52	e52	719.25	758.15	uhf
53	e53	727.25	766.15	uhf
54	e54	735.25	782.15	uhf
55	e55	743.25	782.15	uhf
56	e56	751.25	790.15	uhf
57	e57	759.25	798.15	uhf
58	e58	767.25	806.15	uhf
59	e59	775.25	814.15	uhf
60	e60	783.25	822.15	uhf
61	e61	791.25	830.15	uhf
62	e62	799.25	838.15	uhf
63	e63	807.25	846.15	uhf
64	e64	815.25	854.15	uhf
65	e65	823.25	862.15	uhf
66	e66	831.25	870.15	uhf
67	e67	839.25	878.15	uhf
68	e68	847.25	886.15	uhf
69	e69	855.25	894.15	uhf
70		863.25	902.15	uhf
71		871.25	910.15	uhf
72		879.25	918.15	uhf
73		887.25	926.15	uhf
74	s1	69.25	108.15	vhf 1
75	s2	76.25	115.15	vhf 1
76	s3	83.25	122.15	vhf 1
77		90.25	129.15	vhf 1
78		97.25	136.15	vhf 1
79		104.25	143.15	vhf 1
80	m1	105.25	144.15	vhf 1
81	m2	112.25	151.15	vhf 3
82	m3	119.25	158.15	vhf 3
83	m4	126.25	165.15	vhf 3
84	m5	133.25	172.15	vhf 3
85	m6	140.25	179.15	vhf 3
86	m7	147.25	186.15	vhf 3
87	m8	154.25	193.15	vhf 3
88	m9	161.25	200.15	vhf 3
89	m10	168.25	207.15	vhf 3
90	u1	231.25	270.15	vhf 3
91	u2	238.25	277.15	vhf 3
92	u3	245.25	284.15	vhf 3
93	u4	252.25	291.15	vhf 3
94	u5	259.25	298.15	vhf 3
95	u6	266.25	305.15	vhf 3
96	u7	273.25	312.15	vhf 3
97	u8	280.25	319.15	vhf 3
98	u9	287.25	326.15	vhf 3
99	u10	294.25	333.15	vhf 3

Table 2 FST6 CHANNEL/FREQUENCY-TABLE IF = 38.9 MHz

Fig. 13-8

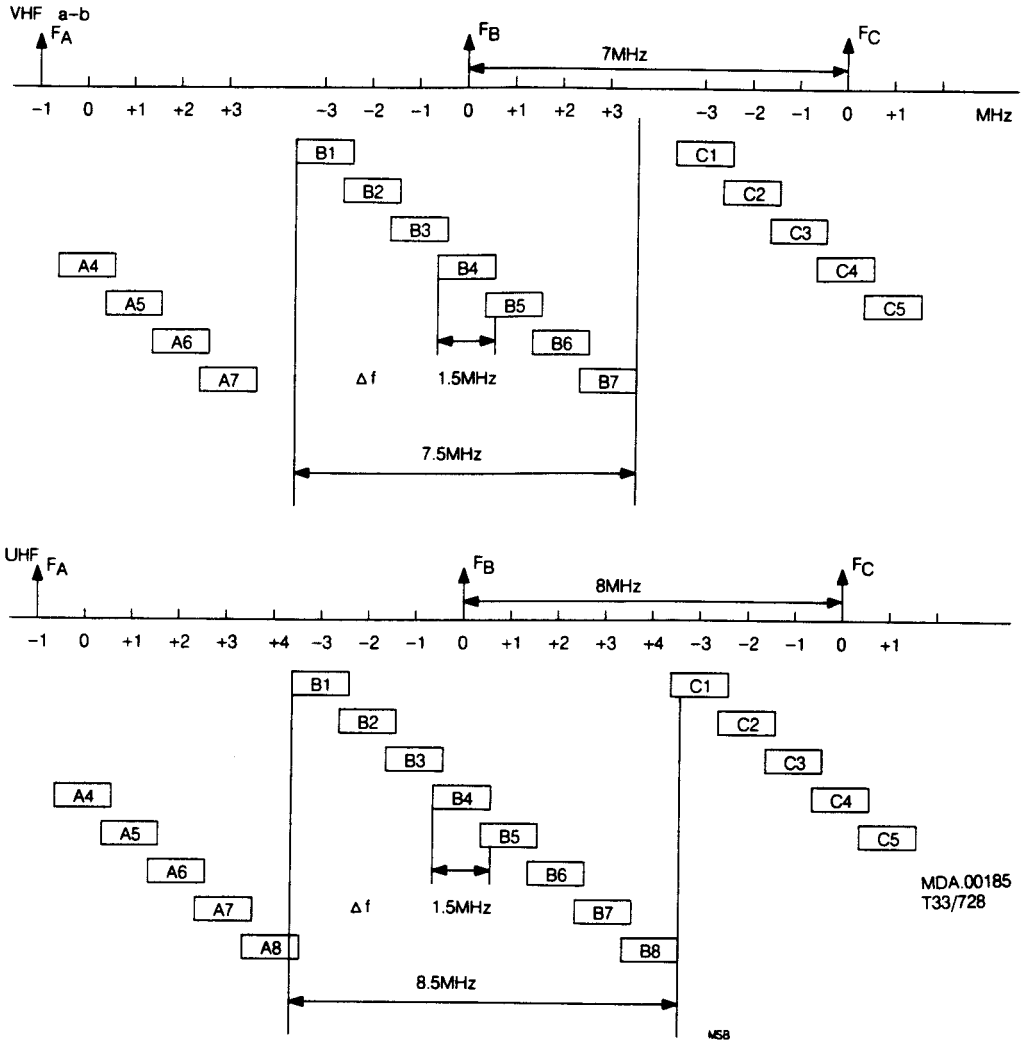


Fig. 13-7

These values can be retrieved via the personal preference (PP) key ( ).
The data of CITAC IC7900 are then via microprocessor IC7830 sent to memories IC7925 and IC7926.
If these preference values are retrieved via the (PP) key, microprocessor IC7830 reads these data out of memories IC7925 and IC7926 and next writes these data from the microprocessor memory to CITAC IC7900.
This enables service to perform an audio-visual check whether the data are stored properly in the memory. In this way the reading and writing operations in the memory are checked when the values of the analogue functions are retrieved.

13.5 Memory drive

Writing into and reading from the external memories takes place via the I²C bus (see appendix 1 for specifications of the bus).
To store a program number it will first be necessary to depress the "store" key (◇). Next the program number is assigned to the channel to which the receiver is tuned. The program number is selected via direct keying or with program number steps via keying of the "step +" and "step –" keys.
These data are stored by depressing the "store execute" key (◇).
After keying of the "store execute" key the program number and the offset frequency in MHz relative to the nominal frequency are stored in the memory.
The data that are via the I²C bus sent to the memories are stored according to the memory map shown in Fig. 13-9.

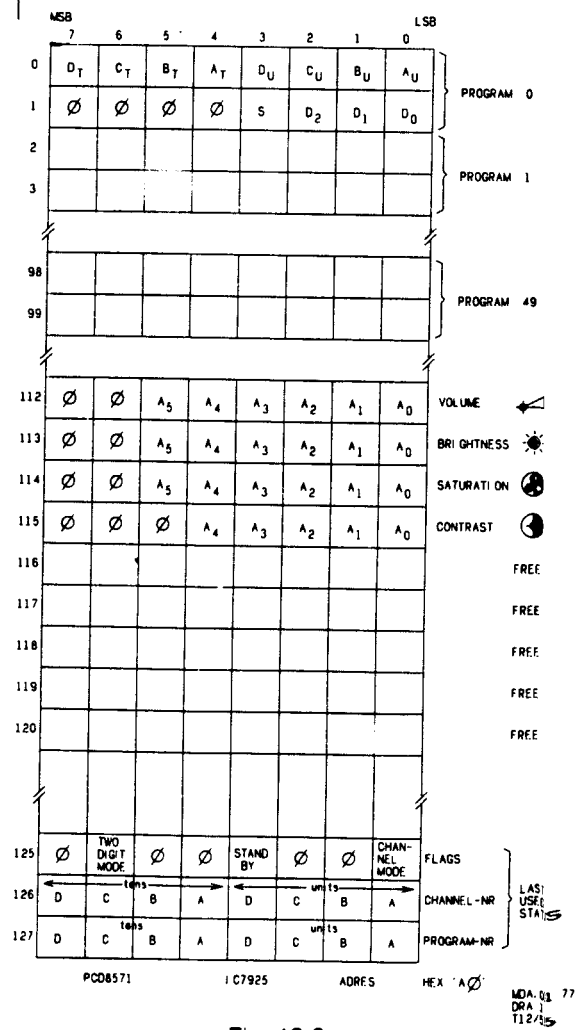
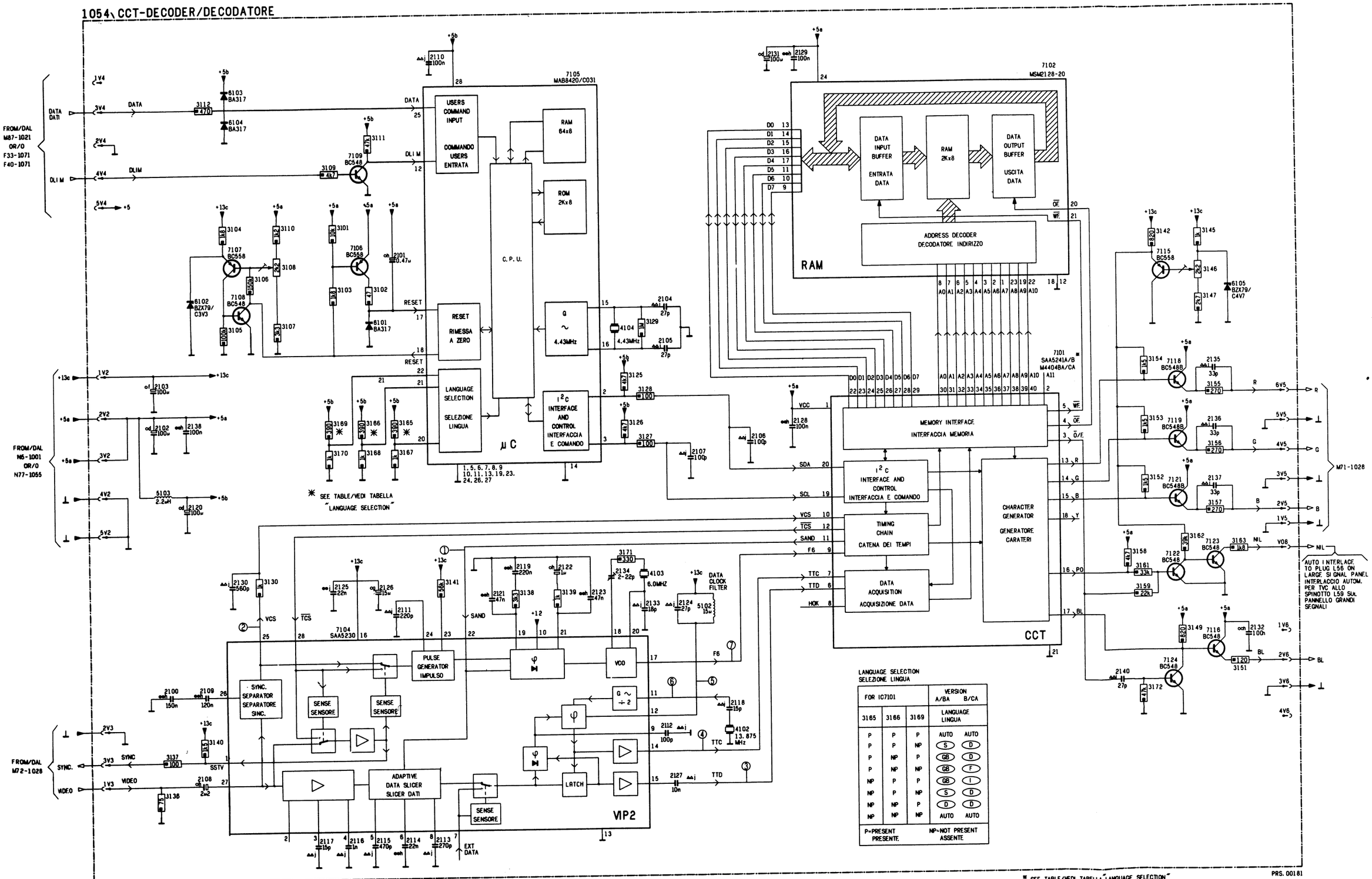


Fig. 13-9

1054\ CCT-DECODER/DECODATORE



LANGUAGE SELECTION
SELEZIONE LINGUA

FOR IC7101			VERSION A/BA	VERSION B/CA
3165	3166	3169	LANGUAGE LINGUA	
P	P	P	AUTO	AUTO
P	P	NP	S	D
P	NP	P	GB	D
P	NP	NP	GB	F
NP	P	P	GB	I
NP	P	NP	S	D
NP	NP	P	D	D
NP	NP	NP	AUTO	AUTO

P=PRESENT PRESENTE NP=NOT PRESENT ASSENTE

① SAND 4.5V 2.5V 0.4V 64µs

② VCS 2.2V 0V

③ TTD 5.4V 2.2V

④ TTC 5.9V 2.2V 6.9 MHz

⑤ CLOCK 5V 13.875 MHz

⑥ CLOCK 12V 6V 13.875 MHz

⑦ F6 6.1V 2V 6.0 MHz

The format for a program or channel selection looks as follows:

	MSB							LSB
0	Dt	Ct	Bt	At	Du	Cu	Bu	Au
	7	6	5	4	3	2	1	0

	MSB							LSB
1	0	0	0	0	S	D2	D1	D0
	7	6	5	4	3	2	1	0

Explanation of symbols used:
DuCuBuAu units of the program/channel number
DtCtBtAt tens of the program/channel number
D2, D1, D0 give the value of the offset for the tuning to the deviating frequency relative to the nominal frequency. S gives the possibility of system selection.
If after storage of a program or channel number, microprocessor IC7830 reads these data from memories IC7925 and IC7926 and sends them to CITAC IC7900, the system will tune to the frequency + offset derived from this program or channel number as if it were a normal program selection.
This enables service to have a visual inspection on the contents of memory IC7925 and IC7926.

This does not work when the set is in the teletext, viewdata or stand-by mode.
The values of the analogue controls are determined by A0-A5 and are stored in the memory (see Fig. 13-9).
The last 3 addresses in the memory are used to store the last mode of the TV receiver before it was switched off. These are the program/channel mode and the program or channel number. If the receiver has been switched to the stand-by mode and then switched off with the mains switch, the receiver will reassume the stand-by mode when it is switched on again.

13.6 Error diagnosis

Part of the program of microprocessor 7830 has been reserved for the service program.
The program of microprocessor 7830 checks itself for errors due to electric interference working on the system with the following measures:
- RAM check
- Password test
- Stack depth test
- Filling up unused ROM space with hex. "FF"
- Protection against endless loops in the software.

If during execution of the program interference nevertheless occurs (e.g. a flash), microprocessor IC7830 generates a hardware self reset via pin 11 of microprocessor IC7830 (see Figs. 13-1 and 13-2).
It drives via transistor 7863 pin 17 of microprocessor IC7830. This informs the microprocessor that a power on reset (POR) takes place and the software will once agian start up the entire system.
The software also generates some error messages if during execution of the program errors are detected in the ICs connected to the I^2C bus.

Survey of possibilities

- RC5 LED signalling. LED D6845 is driven via pin 8 of microprocessor IC7830 when an RC5 command is received at pin 12 of microprocessor IC7830.
- If memory IC7925 or IC7926 does not give an acknowledge to microprocessor IC7830 via the I²C bus, error indication F0 appears on the display.
- If interrupt input, pin 12, of microprocessor IC7830 is constantly low for about 1,3 s, F1 appears on the display. Microprocessor IC7830 will wait software-like in a loop until the interrupt input goes high again.
- If the system is in a TXT mode and the teletext decoder does not give an acknowledge, F2 is displayed by microprocessor IC7830.
- If during 5s no address acknowledge has been received by microprocessor IC7830, via the I²C bus, of various reading and writing actions to CITAC IC7900, error F3 is displayed.

Microprocessor IC7830 continues to send messages to CITAC IC7900 until an acknowledge has been received by microprocessor IC7830.

- A certain check bit pattern is written into the internal RAM of microprocessor IC7830 and read again during system initialization (start) which ordens the data for a program start after a power on reset (POR).
  If an error is found in the RAM now, F4 is displayed.
  Microprocessor IC7830 continues to circulate software-like in an endless loop.
- The possibilities for a visual or an audio-visual check for the working of the reading and writing actions or the contents of memories IC7925 and IC7926 are given in chapters 13.4 and 13.5.
- In the table of Fig. 13-10 a survey is given of error indications with possible error causes.

FAULTDIAGNOSIS CONTROL SYSTEM

Indication on programme display	Indication ⏻	Remark	Incorrect functioning	Correct functioning	Posible defective component
F0					IC7925-IC7926-IC7900
F1					U1840 U1900-IC7830-TS7856
F2		in TXT mode			TXT-decoder
F3					IC7900 +13 supply
F4					U1900-IC7830
88 O.K.			R.C. commands	Local key-board commands	U1840 U1900-TS7856-IC7830
88 O.K.					D6922-IC7900
88 NOT O.K.	LED flickers				U1900-IC7830
88 NOT O.K.					U1900-IC7830 +5 supply

Fig. 13-10

DIAGRAM B

SYNCHRONISATION

HORIZONTAL

EAST-WEST

VERTICAL

SUPPLY

DEGAUSSING

1950 MAINS FILTER PANEL

PRESENT IN /79 SETS

1950 MAINS FILTER PANEL

PRESENT IN /50/57/75 SETS

AUX PANEL

TRANSM IDENT

SCS

ANTI COPY GUARD

START

PROT

50/60Hz

FLYBACK GEN.

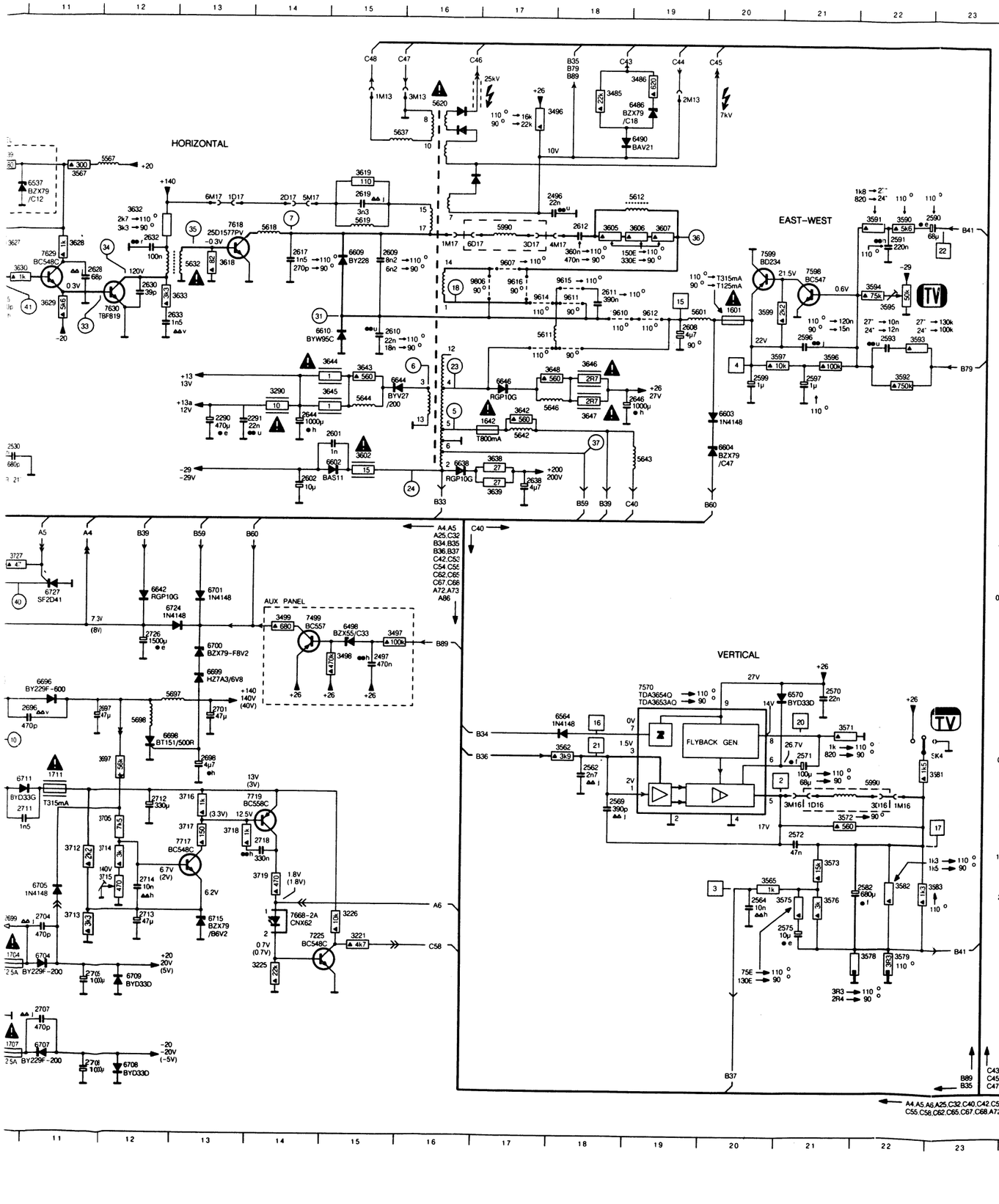
FOR 21"

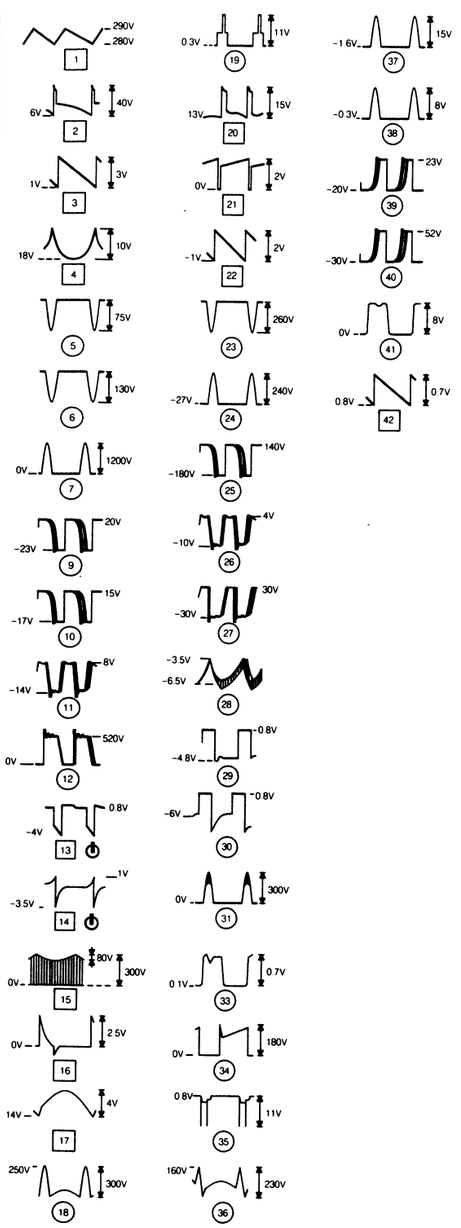
NOT FOR 21"

TO 2699

FROM 2704

* MEASURED IN RESPECT OF (⊥ V)





	1601	D20	3596	E21	7570	I 19
	1642	F17	3597	E20	7598	D21
	1651	H 2	3599	D20	7599	C20
	1651	K 2	3602	F15	7618	C13
	1704	M10	3605	C18	7629	D11
A	1707	N10	3606	C19	7630	D12
	1711	K11	3607	C19	7668-	K 6
	2102	H 3	3618	D13	7668-	M14
	2103	J 3	3619	B15	7685	M 8
	2290	F13	3627	C10	7686	K 8
	2291	F14	3628	C11	7687	J 9
	2496	C17	3629	D11	7717	L13
	2497	I 15	3630	D10	7719	K14
	2530	F10	3632	C12	9607	D17
	2535	B 3	3633	D13	9610	D18
B	2536	B 3	3638	F17	9611	D18
	2539	C10	3639	G17	9612	D19
	2544	A 5	3642	F17	9614	D17
	2545	A 6	3643	E15	9615	D18
	2548	F 5	3644	E15	9616	D17
	2549	A 4	3645	E15	9650	J 6
	2550	F 4	3646	E18	9652	I 6
	2551	E 6	3647	F18	9653	H 6
	2552	E 5	3648	E17	9654	J 6
C	2553	A 8	3650	J 1	9806	D17
	2554	A 8	3651	I 5		
	2555	D10	3652	I 5		
	2560	F 6	3653	J 6		
	2562	K18	3653	I 6		
	2564	L20	3654	H 7		
	2569	K18	3656	I 8		
	2570	J21	3657	J 8		
	2571	J21	3659	K 6		
D	2572	K21	3664	K 9		
	2575	M21	3666	K 5		
	2582	L22	3667	L 6		
	2590	C23	3668	L 7		
	2591	C22	3670	M 9		
	2593	E22	3671	L 8		
	2596	E21	3675	M 5		
	2597	E21	3678	L 5		
	2599	E20	3679	L 6		
	2601	F15	3681	L 7		
E	2602	G14	3683	M 6		
	2608	E19	3684	M 7		
	2609	D15	3685	M 7		
	2610	E15	3686	K 7		
	2611	D18	3687	K 8		
	2612	C18	3689	N 5		
	2617	D14	3690	N 8		
	2619	C15	3691	O 9		
F	2628	D11	3692	O 9		
	2630	D12	3697	K12		
	2632	C12	3699	K 6		
	2633	D13	3705	K12		
	2638	G17	3712	L11		
	2644	F14	3713	M11		
	2646	F19	3714	L12		
	2651	I 2	3715	L12		
	2651	L 3	3716	K13		
G	2653	I 6	3717	K13		
	2654	I 8	3718	L13		
	2655	J 8	3719	L14		
	2656	I 9	3727	H10		
	2657	J 9	3936	F 2		
	2658	I 7	5101	I 3		
	2659	I 10	5555	A 7		
	2664	K10	5567	B12		
	2666	K 5	5601	D19		
	2670	L 9	5611	E17		
H	2675	M 6	5612	C19		
	2681	L 7	5618	C14		
	2683	L 6	5619	C15		
	2690	N 8	5620	A16		
	2691	N 9	5632	D13		
	2694	N 9	5637	B15		
	2696	J11	5642	F17		
	2697	J12	5643	F19		
	2698	K13	5644	F15		
	2699	N 9	5646	F18		
I	2701	J13	5651	H 5		
	2704	M11	5652	J 5		
	2705	N11	5663	H10		
	2707	N11	5687	K 8		
	2708	O11	5697	J13		
	2711	K11	5698	J12		
	2712	K12	5990	C17		
	2713	M12	5990	K22		
	2714	L12	5991	G 5		
J	2718	L14	5992	G 6		
	2726	I 12	6486	A19		
	2936	F 2	6490	B19		
	3221	M15	6498	I 15		
	3225	M14	6535	F 9		
	3226	M15	6537	C11		
	3290	E14	6548	F 5		
	3485	A18	6552	F 3		
	3486	A19	6564	J18		
K	3496	B18	6570	J21		
	3497	I 15	6602	F15		
	3498	I 15	6603	F20		
	3499	I 14	6604	F20		
	3535	A 3	6609	D15		
	3539	B10	6610	E14		
	3541	A 9	6638	F16		
	3542	A 9	6642	H12		
	3543	B 9	6644	E15		
L	3544	B 6	6646	E17		
	3547	F 9	6654	I 8		
	3548	F 4	6655	I 8		
	3549	A 5	6656	I 9		
	3550	F 4	6657	I 9		
	3551	F 3	6664	K10		
	3552	F 3	6666	K 5		
	3554	A 8	6667	L 5		
	3555	C10	6668	L 6		
	3557	F 7	6670	L 9		
M	3558	F 7	6671	L 9		
	3559	F 7	6672	L 8		
	3560	F 7	6675	L 5		
	3561	F 7	6686	K 8		
	3562	J18	6689	M 5		
	3564	F 8	6690	N 7		
	3565	L20	6696	I 11		
	3566	F 9	6698	J13		
	3567	B11	6699	I 13		
N	3571	J21	6700	I 13		
	3572	K21	6701	H13		
	3573	L21	6704	M11		
	3575	L21	6705	L11		
	3576	L21	6707	O11		
	3578	M22	6708	O12		
	3579	M22	6709	N12		
	3581	K23	6711	K11		
	3582	L22	6715	M13		
O	3583	L23	6724	H13		
	3590	C22	6727	H11		
	3591	C22	6935	F 2		
	3592	E22	7225	M14		
	3593	E22	7499	I 14		
	3594	D22	7550	B 9		
	3595	D22	7551	F 3		

DIAGRAM A

1850 1840 1900

I.R. TRANSM. I.R. RECEIVER

OPERATING PANEL FST

CITAC CIRCUIT

7830 MAB8461/W051

DATA PROC

MEMORY MEMORY

PICTURE CARRIER IDENTIFICATION

AFC TEST

FREQUENCY BUFFER

REFERENCE COUNTER FREQUENCY COUNTER

SELF RESET POWER ON RESET

STATUS SCART

EXTERNAL SCART-STATUS EXTERNAL

5V SUPPLY

CHASSIS 2B

B+C

PRS 02617
T33-726

CS 9 472

1840	A 4	7900	B17
1850	A 1	7906	G18
1867	G 9	7908	G17
1921	F13	7925	B12
1925	C12	7926	B13
2733	M15	7938	H13
2734	L15		
2735	K17		
2736	J18		
2842	D 9		
2843	D 9		
2867	F10		
2868	G10		
2871	M 9		
2872	M 9		
2873	N 9		
2909	F17		
2918	H15		
2921	G14		
2922	I 16		
2925	B11		
2929	F12		
2935	F12		
3220	M13		
3729	L14		
3730	K14		
3731	K15		
3732	L14		
3733	M15		
3734	J13		
3735	J16		
3736	M15		
3737	N16		
3738	K16		
3739	M17		
3740	M16		
3741	L18		
3742	L17		
3836	L 5		
3837	L 4		
3838	K 3		
3842	D10		
3843	C10		
3845	J 4		
3846	K 5		
3847	J 5		
3853	A 8		
3854	B 8		
3855	A 7		
3856	B 5		
3857	B 5		
3858	B 6		
3861	I 9		
3862	I 10		
3863	H10		
3867	G10		
3871	N10		
3873	C 3		
3874	C 4		
3875	D 5		
3876	D 5		
3877	K 3		
3878	L 3		
3879	E 5		
3880	E 5		
3881	F 5		
3882	F 5		
3883	G 5		
3884	G 5		
3885	H 5		
3886	H 5		
3891	M 2		
3892	M 2		
3893	N 2		
3894	M 5		
3895	M 6		
3905	G18		
3906	H18		
3907	G18		
3908	G17		
3909	F18		
3911	C11		
3912	D11		
3915	C17		
3916	C17		
3917	C17		
3918	H17		
3919	H15		
3922	I 16		
3923	I 17		
3925	B12		
3926	D12		
3927	C12		
3929	I 15		
3930	I 14		
3931	I 15		
3932	I 14		
3935	F11		
3938	H13		
3939	H14		
3940	H13		
3944	B16		
3946	B17		
3947	D17		
3948	D17		
3949	D17		
6729	M13		
6730	M14		
6731	K14		
6733	J15		
6734	J12		
6739	M18		
6741	L17		
6742	M16		
6837	M 4		
6838	M 4		
6845	J 4		
6863	I 9		
6886	C 1		
6887	D 1		
6891	M 2		
6892	M 2		
6893	N 2		
6922	I 16		
6925	B12		
6932	A15		
6944	B16		
7731	J14		
7735	J17		
7736	M15		
7738	K17		
7742	L15		
7830	C 8		
7831	D 1		
7845	J 5		
7853	A 8		
7856	B 5		
7863	H10		
7874	C 3		
7875	D 5		
7877	L 3		
7894	M 5		

DIAGRAM C

CHANNEL SELECTOR

IF AMPL.+DET.+AGC+AFC

CHROMINANCE+LUMINANCE

1015
FE618Q
FE644Q

TDA2545A

TDA2541

AUDIO

VIDEO

RF-AGC

DIV :256

VHFa VHFb HYPERBAND UHF

V_{VARI} 0→32V

1300
CHROMINANCE DECODER

CVBS

7300
TDA4580/V2

VIDEO CONTROL

PAL/NTSC

BLANKING

MATRIX

CUT-OFF CONTROL

1400
R-G-B AMPLIFIER

1750
TXT-DECODER

1100
STEREO DECODER

U829B 5.5MHz

U829B 5.74MHz

TDA3803
MATRIX + IDENTIFICATION

HEF4053

TDA3810
MONO STEREO SPATIAL

TDA1524A

HEF4011
HEF4012

BC548 MUTE

SOUND

7220 TDA1520B

7210 TDA1520B

A+B

A2, A16
A17, A19
A20, A24
A26, A27
A28, A31
A57, B42
B58, A61
A80, A81
A82, A83
A84, A85

C30.C90

A26, A27
B40
B42, B54
B58, A61
A80, A81
A82, A83
A84, A85

C51

A21 A22
B43, B44
B45, B46
B47, B48
C49, B65

43 44 45 46 47 48 49 50 51 52 53 54 55 56

CHROMINANCE+LUMINANCE

7300
TDA4580/V2

VIDEO CONTROL

PAL/NTSC

BLANKING

MATRIX

CUT-OFF CONTROL

MATRIX

TXT-DECODER

1400

R-G-B AMPLIFIER

SEE SERVICE MANUAL "REMARKS"

1100
STEREO DECODER

U829B 5.5MHz

U829B 5.74MHz

TDA3803
MATRIX + IDENTIFICATION

HEF4053

TDA3810
MONO STEREO SPATIAL

TDA1524A

HEF4011
HEF4012

BC548 MUTE

SOUND

7220 TDA1520B

7210 TDA1520R

1250

CHASSIS 2B

PRS 02616
T-33/733

CS 9 474

	1015	B 1	3468	C28
	1100	K13	3469	A19
	1224	K24	3470	D29
	1250	L30	3471	F30
	1300	B 8	3472	G29
A	2020	F 1	3473	G29
	2021	F 2	3474	G29
	2022	F 3	3477	G20
	2023	B 2	3479	F27
	2024	F 2	3480	F27
	2025	F 3	3481	H26
	2027	F 4	3488	A16
	2028	E 4	3489	I 28
	2030	B 5	3490	I 27
	2200	L22	3491	H28
B	2201	K23	3492	H27
	2202	L23	3493	B15
	2203	L24	3495	I 25
	2204	O22	3506	G15
	2205	L21	3507	G15
	2210	N22	3508	G15
	2211	M23	3509	K 7
	2212	O23	3510	L 7
	2213	N24	3513	K 7
	2215	N21	3514	K 6
C	2220	M21	3515	K 6
	2221	L21	3516	L 6
	2222	K26	3519	I 7
	2280	D13	3520	J 6
	2281	C13	3521	J 7
	2283	F13	3522	F 7
	2284	F13	3523	I 7
	2285	E13	5027	F 4
	2289	G19	5465	F29
D	2293	B17	5466	F28
	2295	G17	5995	O26
	2297	B17	5996	O27
	2300	B19	5997	O28
	2301	B19	5998	O29
	2302	B20	6418	A27
	2400	A22	6438	D27
	2402	A26	6458	G26
	2403	B25	6462	H28
	2422	D25	6481	E27
E	2423	E25	6481	H27
	2433	I 25	6488	B15
	2442	F25	6491	I 27
	2443	G24	6492	H27
	2462	I 26	6503	N 9
	2463	G28	6504	M 9
	2466	A29	6505	L 9
	2470	D28	6506	L 9
	2471	G30	6508	K 7
F	2477	G20	6510	L 7
	2481	E27	6512	L 7
	2481	G27	6518	I 7
	2491	C27	6519	I 7
	2508	K10	7210	M23
	2514	M10	7220	O23
	2515	L 9	7223	K27
	2517	L10	7224	K25
	2520	F 7	7300	B13
	2522	N10	7402	B26
G	2523	M 9	7412	C25
	2537	I 7	7413	C26
	2538	G 8	7418	B27
	3023	B 3	7422	D25
	3030	B 6	7432	E24
	3032	G 7	7433	E25
	3033	F 5	7438	D26
	3200	L22	7442	G25
	3201	L22	7452	H24
H	3203	L23	7453	H25
	3204	K22	7458	G26
	3205	K22	7465	H25
	3206	L24	7479	B27
	3207	L24	7480	E26
	3210	N22	7481	H26
	3211	O22	7488	A15
	3213	O23	7489	I 28
	3214	M22	7520	G 6
	3215	N22	SK2	G15
I	3216	N24		
	3217	O24		
	3222	K26		
	3223	K26		
	3224	K25		
	3240	L27		
	3242	L27		
	3291	B20		
	3292	A17		
J	3293	B17		
	3294	G17		
	3295	H17		
	3296	A16		
	3297	B16		
	3399	A22		
	3400	A22		
	3401	A25		
	3402	A25		
	3403	B25		
K	3404	B24		
	3406	B24		
	3407	B24		
	3408	C24		
	3409	C23		
	3410	C24		
	3412	B25		
	3413	C25		
	3414	C23		
	3416	A26		
L	3418	A27		
	3419	C27		
	3421	D24		
	3422	D25		
	3423	D24		
	3424	E24		
	3426	D24		
	3427	E23		
	3428	E23		
M	3429	E23		
	3430	F23		
	3432	E24		
	3433	F25		
	3434	E22		
	3436	D26		
	3438	D26		
	3439	E27		
	3441	F24		
N	3442	F24		
	3443	G24		
	3444	G23		
	3446	G23		
	3447	G23		
	3449	H23		
	3450	H23		
	3451	H22		
	3452	H24		
O	3453	H24		
	3454	H22		
	3455	H22		
	3456	F25		
	3458	F26		
	3459	F27		
	3463	H26		
	3465	H25		

PART II (Computer Controlled Teletext)

1. INTRODUCTION

1.1 Characteristics of CCT

Computer Controlled Teletext (CCT) constitutes a new (second) generation teletext decoders with more possibilities than first-generation decoders. Examples of these possibilities are:

- **Reception of so-called ghost rows.**
  Ghost rows are additionally transmitted teletext rows which contain supplementary page information. The rows are invisible to first-generation teletext decoders, which explains the name.
- **Automatic change of the character set** in case of reception of other languages. A CCT decoder can contain the character sets of three languages.
  In the first-generation decoders a change of character generator IC was necessary to change language.
- **Multipage Acquisition.** This is the searching for and storing of several pages simultaneously, so that waiting times are reduced.
- **Improved display properties.** For character reproduction, use is made of a 12 × 10 dot matrix instead of the 6 × 10 matrix instead of the 6 × 10 dot matrix of the first-generation decoders.
- **Display of a so-called status row.** The system generates one additional row above or below the main text, which contains status information of the decoder.

The design of the CCT decoder is such that the functions that are fixed by the broadcast specifications and that must always be performed in the same way, such as the generation of sync signals and the decoding of teletext signals, are carried out by special circuits inside the ICs of the decoder. The functions that are liable to differ significantly between different applications, such as the generation of status information and the translation of operation commands, are performed by the associated microcomputer.

1.2 Block diagram TIC TAC TROM decoder

The CCT decoder is the successor and substitute of the well-known TIC TAC TROM decoder. As this description makes frequent comparisons with the working of the first-generation decoder, some knowledge of that decoder is required. In this section only a brief description of the block diagram of the TIC TAC TROM decoder is given.

The block diagram of the TIC TAC TROM decoder is shown in Fig. 1.1.

The basic decoder functions are performed by:

- **VIP** (Video Input Processor) SAA5030, a linear IC which provides serial data and clock derived from the incoming video signal. It also arranges timing synchronisation for the rest of the decoder.
- **TAC** (Teletext data Acquisition and Control) SAA5040 arranges the capture of the requested page into memory. The IC is also concerned with the overall decoder control and writing user status information into memory.
- **MEMORY** 1K bytes of RAM (Random Access Memory) for page storage.
- **MEMORY INTERFACE** standard LS-TTL ICs as interface for memory addressing.
- **TROM** (Teletext Read Only Memory) SAA5052.
  This character generator provides the TV with R, G and B signals for displaying the text on the screen.
- **TIC** (Timing Chain) SAA5020.
  Provides the timing and addressing signals for the whole decoder.

The TIC TAC TROM decoder is a so-called single-page decoder, in which **one** page is requested and searched for at a time.
As soon as the page is found, it is displayed on the screen. A next page can then be requested and searched for.

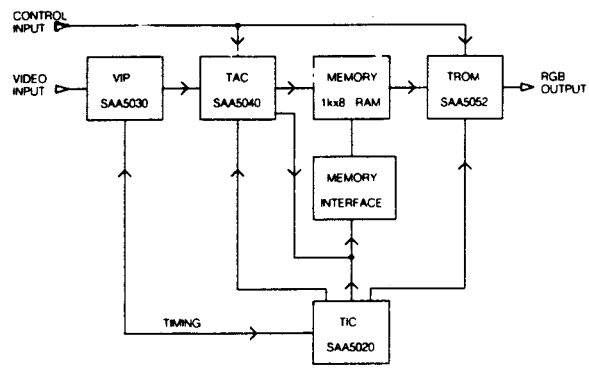


Fig. 1.1

PRS 00755
T-26/605

1.3 Block diagram CCT decoder

The general block diagram of the CCT decoder is shown in Fig. 1.2.

The heart of the circuit consists of the CCT IC, type SAA5240. CCT means Computer Controlled Teletext.
The CCT IC replaces TIC, TROM, memory addressing and part of the TAC in the first-generation decoder.
The processing of control commands and status functions, previously carried out by the TAC, is now performed by a control microcomputer. The control functions of this microcomputer may either be accommodated in the microcomputer of the control system of the TV or in a separate computer in the teletext decoder itself.
The interface between the microcomputer and the CCT IC is the standard IIC bus. This bus is used bidirectionally. However, most data flow is from the microcomputer to the CCT IC. Via the bus and the CCT IC the microcomputer can read data from the page memory.
The page memory consists of standard static RAM and is connected with the CCT IC. 1K x 8 bits of memory are required per page (1K = 1024 bits). A maximum of 8K x 8 bits of memory can be connected for the storage of 8 pages in normal mode or 4 pages in ghost-row mode. The program in the microcomputer must be suitable for the available capacity and the desired mode. So the connection of extra memory alone does not automatically lead to more stored pages.

The functions of the videoprocessor are performed by VIP2 (SAA5230). This Video Input Processor is, in fact, a redesigned VIP1 (SAA5030) with improved reception of teletext information under poor signal conditions. VIP2 does not contain any frequency-critical external components. VIP1 and VIP2 are not interchangeable.

Many variants of CCT-based decoders can be composed by either using or ignoring the extra possibilities of the CCT concept. The CCT decoder discussed in this description is the functional substitute of the TIC TAC TROM decoder for application in, for example, system 4 TV sets.
The CCT teletext panel has the same dimensions and the same plug positions as the TIC TAC TROM decoder. Furthermore it uses the same input and output signals and supply voltages. In summary:
- Control commands are given with MIBUS signals (MIBUS = MULLARD INSTRUCTION BUS);
- The composite video signal CVBS (CVBS = Composite Video Blanking Sync) is used as information source;
- Teletext information is provided in the form of R, G and B signals (R, G, B = Red, Green, Blue);
- Blanking of the TV picture is carried out by a separate blanking signal (BLAN);
- Interlacing can be switched on and off with a separate NIL signal (NIL = No Interlace).
- Supply voltages are +5 V and +12 V.

To be able to use the CCT decoder, The RC-5 remote control transmitter must be provided with the extra control command "Next Page". Furthermore the processor in the control system must be capable of transmitting this function to the decoder via the MIBUS lines. A requested page is displayed on the screen only after a "Next Page" command has been given.

In Fig. 1.3 the block diagram of the system 4 CCT decoder is shown. Compared with the general block diagram, this block diagram has been supplemented with input and output circuits to adapt the signal levels and impedances of applied and transmitted signals. To control the decoder and to convert the MIBUS signals into IIC commands, use is made of the microcomputer, MAB8420/C031.
The program in the microcomputer supports multipage activity of the decoder.
The memory of the decoder is formed by memory IC MSM 2128-20. In this IC, which has a capacity of 2K bytes, the information for two teletext pages can be stored.
The memory can be divided into a foreground memory and a background memory. The foreground memory displays the first requested page on the screen. This page is being refreshed while the background memory is searching for the next page. The number of this next page can either be taken from a preset list that the user has stored in a memory, or it can directly be stated by the user. As soon as the "Next Page" key of the remote control transmitter (eg. RC5373) is depressed, the memory functions will be exchanged: the background memory becomes the foreground memory, so that the contents of this memory are displayed on the screen. The foreground memory becomes background memory and will be available for searching for a next page.

1.4 Circuit diagram CCT decoder

The circuit diagram of the system-4 CCT decoder is shown in Appendix C. The circuit consists of only four ICs and several input and output circuits. The inputs and outputs of the ICs are often directly connected with one another, that is, without additional components. The following chapters enter into the various ICs and buffer circuits.

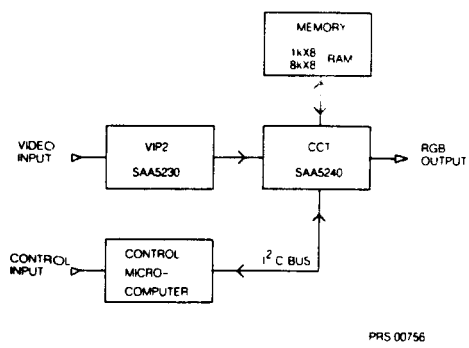


Fig.1.2

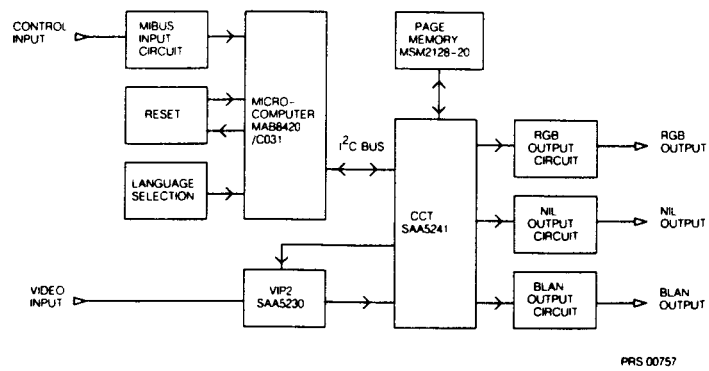


Fig. 1.3

2. VIDEO INPUT PROCESSOR VIP2

2.1 Block diagram

The Video Input Processor, version 2 (VIP2, SAA5230) is an improved version of VIP1 (SAA5030).
VIP2 does not use any critically adjusted components for the acquisition of the teletext data from the video signal.
The IC performs three main functions:

1. Acquiring the teletext data from the CVBS signal and regenerating the data clock;
2. Generating a 6 MHz display clock;
3. Providing synchronisation signals for teletext display.

Figure 2.1 shows the block diagram of VIP2.
The data slicer circuit extracts the teletext information from the composite video signal of the TV receiver and applies this information to the CCT-IC in the form of the teletext data signal (TTD).
Using a crystal frequency (13.875 MHz), the clock regenerator circuit generates the teletext data clock TTC (Teletext Clock) that is synchronized on the TTD signal. This clock is also applied to the CCT-IC.
The 6 MHz Clock Oscillator generates the 6 MHz display clock signal F6 that is used as time basis for the teletext information display.
The Clock Oscillator is controlled by the phase detector circuit by means of synchronisation signals from Sync Separator Circuit and CCT-IC. These sync signals are used to synchronize the F6 clock to the incoming video signal.
The Clock Oscillator applies the F6 clock signal to the CCT–IC and CCT-IC in turn returns the SAND synchronisation signal to the Phase Detector Circuit. In this way the Phase detector, 6 MHz Clock Oscillator and CCT-IC form a closed loop. The synchronisation circuit extracts the composite sync signal (VCS) from the CVBS signal and passes it on to the timing chain section of the CCT IC. The circuit can furthermore transmit a composite sync signal (TCS) from the CCT-IC to the time basis of the TV receiver for synchronisation of the TV picture in teletext mode.
The signal transfer between VIP2 and the Timing Chain function of the CCT–IC is discussed in section 4.5 (Timing Chain function).

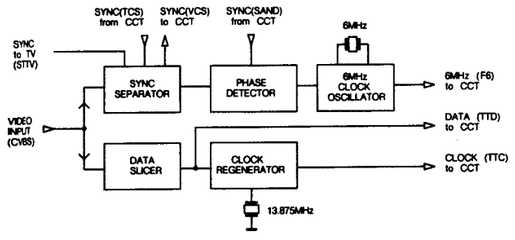


Fig. 2.1

2.2 Circuit diagram

The circuit diagram of VIP2 is shown in Fig. 2.2.
The composite video signal is applied to pin 27 of IC7104 via coupling capacitor C2108. R3136 is a terminating resistance for the coaxial cable with which the video signal is supplied from the luminance circuit of the TV receiver. In the VIP, the DC-separated video signal is applied to a sync separator and to switch A, which both form part of the sync separator circuit, and to an amplifier stage which forms part of the data separator – clock generator circuit.

The amplification of the stage can be adjusted to two values by means of a logic level on pin 2 of the VIP.
When pin 2 is LOW, the input signal level is allowed to be about 1 V (video signal sync white between pin 27 and ground). When pin 2 is HIGH, the input signal level is allowed to have a peak-to-peak value of 2,5 V. If pin 2 is not connected, the input is high.
In either case the sync amplitude must not exceed 1 V (peak-to-peak). Furthermore the HF losses in the video signal are compensated in the amplifier stage. The capacitor at pin 3 filters the video signal for the HF compensator. The HF amplitude is stored in the capacitor at pin 4.

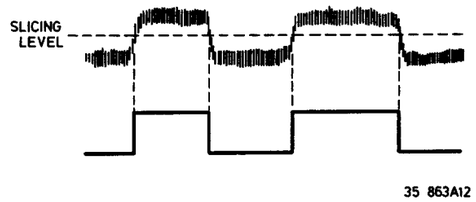


Fig. 2.3

The video signal coming from the amplifier stage is applied to the adaptive data slicer circuit. This circuit cuts the signal off at half the amplitude to eliminate noise and interference voltages that are superposed on the signal. The effect of these voltages is smallest at half the signal amplitude. See Fig. 2.3.

The data slicer uses the external capacitors at pins 5, 6 and 8 of IC7104 (C2115, C2114 and C2113, respectively).
The black level is stored on pin 6 and the amplitude of the video signal on pin 5.
From these two signals the slicing level is determined.
1,5 µs after the start of the line sync pulse the data slicer is switched off for 7 µs by the CBB part of the SAND pulse (see Fig. 2.4).
This is done to avoid that the colour burst of the video signal interferes with the working of the data slicer.
The capacitor at pin 8 determines the timing of the data slicer.

After the sliced video signal has been squared up, it can be clocked in the latch via switch C and can be output, as the TTD signal, via an amplifier output buffer on pin 15.
Switch C is operated by an external digital signal applied at pin 7, for example from an echo compensator. The sence C circuit at pin 7 detects the presence of an external signal and, in that case, changes switch C over. If pin 7 is not connected, the signal from the data slicer is passed on to the latch. This latch is clocked by the teletext clock (TTC) which is generated by a free running crystal oscillator and whose frequency is twice (13.875 MHz) the transfer speed of the teletext signal (6,9375 Mbit/s). After division by two this frequency is synchronized to the sliced data signal by means of a phase-shifting network and a phase detector. The phase found by the phase detector is "stored" in capacitor C2112 at pin 9.

The applied circuit for regenerating the clock signal finds the correct clock phase before the end of the clock run-in which is transmitted at the beginning of each teletext row. The regenerator applied here does not use any critically adjusted components. The data clock filter of the phase shifter at pin 12 consists of S5102 and C2124, both with a fixed value.
The output signal of the phase shifter is fed outside via an output buffer on pin 14. Both the TTD and the TTC signal are output with reduced slopes and amplitudes to diminish the chance of interferences with other parts of the TV receiver as much as possible. The video composite sync signal VCS is extracted from the composite video signal on pin 27 by means of a sync separator circuit. The black level of the video signal is stored in capacitors C2100 and C2109 at pin 26. The VCS signal is available at pin 25 and is applied via the RC filter R3130/C2130 to the timing chain section of the CCT-IC for frame synchronization of the teletext display.

The $\overline{TCS}$ (Text Composite Sync) signal is applied from the CCT-IC to pin 28 of VIP2. Then the $\overline{TCS}$ signal can be output on pin 1, via switch A and the buffer circuit, as sync signal for the TV receiver. Switch A is changed over by the sense A circuit when the presence of the $\overline{TCS}$ signal is detected on pin 28.
With a resistor from pin 1 to ground or to +12, positive or negative sync can be chosen on pin 1.
The $\overline{TCS}$ signal can be switched off under the control of the IIC bus commands. The result of this is that the TCS line gets a higher level than the normal voltage. This condition is detected by the sense A circuit which then changes switch A over. The composite video input signal on pin 27 is now passed on, via switch A and the buffer, to pin 1 for synchronization of the normal TV picture.

The 6 MHz display clock F6 is generated by a VCO (Voltage Controlled Oscillator). The nominal frequency of the VCO (6MHz) is determined by the series resonance circuit between pins 18 and 20. This circuit consists, among other things, of ceramic resonator KT4103 and trimmer C2134. The VCO is controlled by a phase detector which compares the SAND signal with the pulses formed by the pulse generator circuit from the VCS or $\overline{TCS}$ sync signal.

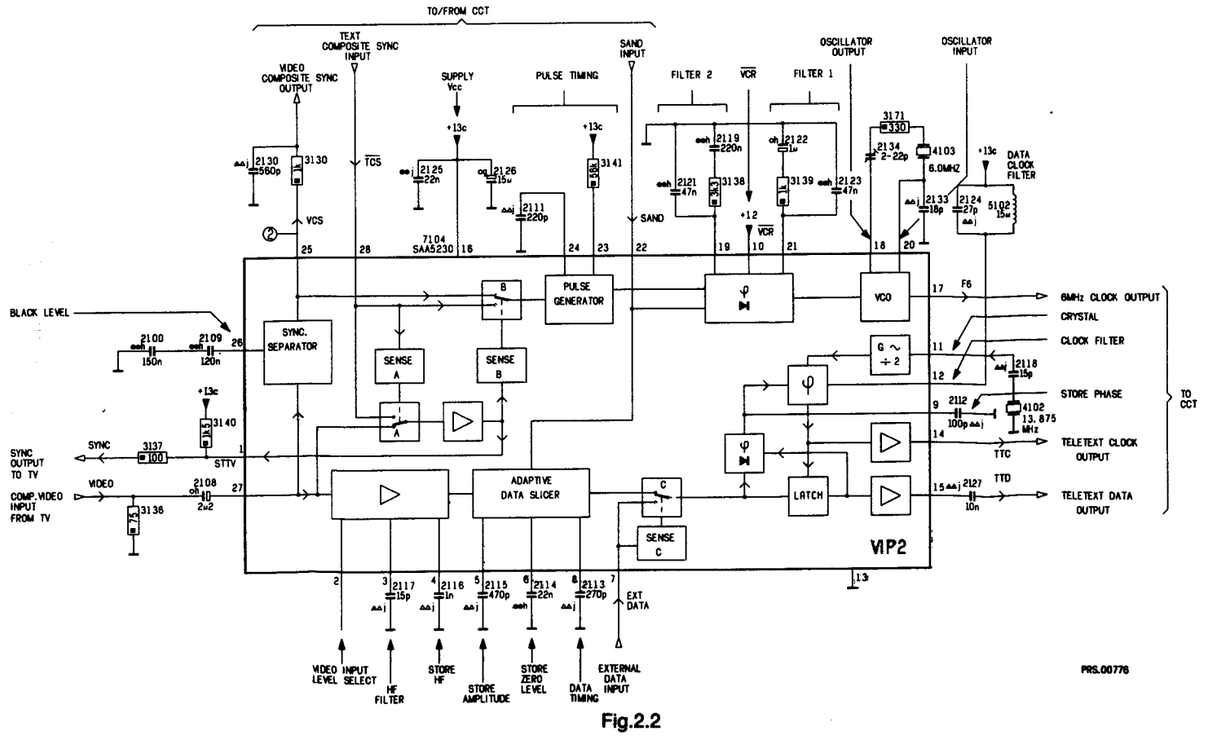


Fig.2.2

The phase detector is equipped with two external filters: filter 1 between pin 21 and ground has a long time constant for the line phase detector; filter 2 between pin 19 and ground has a short time constant for lock-up of the Phase Locked loop and for use in video recorder mode. With a logic low level at pin 10 ($\overline{VCR}$) the short time constant can be switched on permanently to synchronize teletext to a videorecorder signal. If the input is left open, it has a logic high level.

From the CCI-IC the SAND signal is applied to pin 22. The signal shape and the timing of the SAND signal in relation to the composite video signal CVBS is shown in Fig. 2.4.

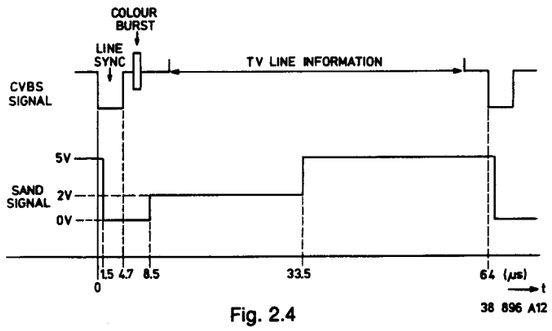


Fig. 2.4

In the CCI-IC, the SAND signal is composed from two line frequency signals: Colour Burst Blanking (CBB) and Phase Lock (PL). The PL part of the SAND signal is used to lock the F6 signal in phase with the video signal. The CBB part is used to switch off the data slicer so as to avoid that the colour burst in the video signal disturbs the working of the data slicer.
If the signal quality detector from the CCT-IC detects a poor signal quality of the teletext signal, the PL component will be removed from the SAND signal, causing the 6 MHz oscillator to become free-running.
The pulse generator circuit feeds control pulses to the phase detector. These control pulses are either formed from the VCS or from the TCS synchronisation signal, depending on the position of switch B.
Switch B is operated by the sense B circuit with the aid of the DC level at pin 1 of VIP2 (STTV).
If pin 1 is not connected, its DC level is such that switch B changes over to the position other than the one shown in Fig. 2.2. In that case the 6 MHz oscilllator will be synchronized to the signal that is applied to pin 28.
If pin 1 has been connected, however, the 6 MHz clock will be synchronized with the Video Composite Sync (VCS) signal that is extracted by the sync separator from the applied video signal. In normal teletext applications the 6 MHz clock is synchronized to the VCS signal.

The VIP IC is power supplied from 12 V between pin 16 (+) and pin 13 (ground).

3. THE MICROCOMPUTER CIRCUIT

3.1 Introduction

The CCT decoder is controlled by microcomputer IC7105 (MAB 8420/C031).
The functional structure of this IC is shown in Fig. 3.1

The microcomputer contains a Central Processing Unit (CPU) a program store (ROM = Read Only Memory), a working store (RAM = Random Access Memory), a crystal oscillator, an IIC interface and several input and output circuits.

3.2. CPU and Memory

The CPU processes data on the basis of the program stored in ROM. This ROM has a capacity of 2K x 8 bits (2048 bytes) and is what is called "mask programmed". This means that the program has been applied during the production of the IC and that it cannot be changed any more. The internal working store (RAM) is a dynamic memory with a capacity of 64 x 8 bits (64 bytes).

3.3 Oscillator and clock

The crystal oscillator generates the clock frequency for the microcomputer. The frequency-determining components of this oscillator are connected between pin 15 (XTAL 1) and pin 16 (XTAL 2). The frequency of the oscillator is 4.43 MHz, but can, in principle, be chosen freely. It is also possible to apply an externally generated clock signal as frequency reference to the XTAL 1 input (pin 15) (for example for testing purposes).
For an adequate refreshing of the dynamic logic of the microcomputer the oscillator frequency must be higher than 600 kHz.

If the crystal oscillator does not work, the CCT decoder will not react to control commands relating to teletext: teletext mode cannot be switched on and there is no activity on the IIC bus.

3.4 IIC interface

The IIC interface arranges that information from the CPU is transmitted via the IIC bus in conformity with the relevant procedures, and that information that is applied via the bus is received and made suitable for processing in the CPU. The interface is also responsible for address recognition.
The IIC bus consists of two lines: SDA (Serial Data) at pin 2 and SCL (Serial Clock) at pin 3.
More detailed information on the IIC bus is given in Appendix A.

3.5 Operation

The microcomputer receives control commands from the television control system in the form of the MIBUS signals DATA and DLIM (pin 25 and pin 12, respectively). The control commands relating to teletext are processed and translated into signals according to IIC bus format and are then passed on, in the form of the signals SDA and SCL (pin 2 and pin 3, respectively) to the CCT-IC via the IIC bus. The control commands are transmitted to the microcomputer on an interrupt basis.

3.6 Language selection

The microcomputer has 3 inputs (pin 20, 21 and 22) that are used for the so-called language selection.

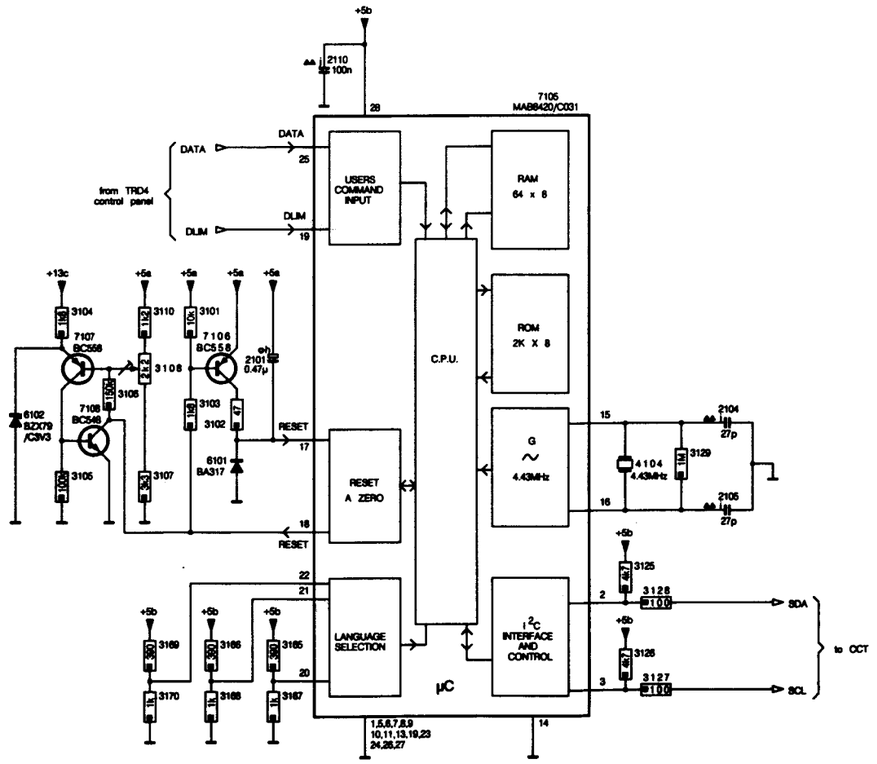


Fig. 3.1

PRB.02788
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Language selection enables the character set of the decoder to be changed such that it contains the special characters that are used in a specific language. For example: German language ä, ö, ü, ß, English language $, ½, ¼. In the first-generation decoders a specific character generator IC (TROM) had to be used for a specific language. To change the character set, the TROM IC had to be changed.

In the CCT decoder, logic levels at the language selection inputs are used to make a choice from three different character sets (languages). The information on the desired language is transmitted to the CCT-IC via the IIC bus. For, the character sets are accommodated in the character generator of the CCT-IC.

The logic levels on the language selection inputs are determined by means of resistors R3165 to R3170. When all resistors have been applied, the inputs are connected with a voltage divider between +5b (5 V) and ground. The voltage on the divider is about 3,6 V, which corresponds to a logic high level. A logic low level at an input is obtained by removing the resistor to +5b. The pull-up resistors are vertically (erect) mounted on the PCB to facilitate their removal (cutting loose).

The selection table for pull-up resistors R3165, R3166 and R3169 for the various languages is shown in Fig.3.2.
When all pull-up resistors are present, automatic language selection (auto) is possible. In that case the character set is determined by the control bits C12, C13 and C14 from the page header of the teletext page.
The transmitter itself can change over to the set with language specific characters belonging to the transmitted text. If automatic language selection is not desired, or if it is not yet used by the transmitter, a character set can be selected by removing one or more pull-up resistors as shown in Fig. 3.2. If automatic language selection is wanted again in a later stage, it can simply be chosen by removing all pull-ups.

LANGUAGE SELECTION

FOR IC7101			VERSION A/BA	VERSION B/CA
3165	3166	3169	LANGUAGE	
P	P	P	AUTO	AUTO
P	P	NP	(S)	(D)
P	NP	P	(GB)	(D)
P	NP	NP	(GB)	(F)
NP	P	P	(GB)	(I)
NP	P	NP	(S)	(D)
NP	NP	P	(D)	(D)
NP	NP	NP	AUTO	AUTO
P=PRESENT			NP=NOT PRESENT	

Fig.3.2 PRS.00760

There are two versions of the CCT-IC: SAA5241A (M4404BA) with the specific characters for English, Swedish and German, and SAA5241B (M4404CA) with the characters for German, French and Italian.

A more detailed description of the language selection inside the CCT–IC is given in section 4.6.

3.7 Reset

The microcomputer is reset by a high level at pin 17. The circuit at pin 17 and pin 18 is responsible for the reset in the following cases:
- After switch-on of the supply voltage (Power On Reset).
- In case of a too low voltage of the +5a power supply (voltage guard).
- After a reset pulse from the microcomputer itself at pin 18 (self-reset).

3.7.1 Power On Reset

After switch-on of the supply voltage, the microcomputer is set to a defined initial state by means of a hardware reset at pin 17. The reset circuit is powered by the +5a (5 V) and the +13c (12 V) power supply. After switch-on, the +5a and +13c voltages increase quickly. The voltage on e- TS7107 soon reaches the Zener voltage of D6102 (3,3 V). The voltage on the slider of R3108 is part of the +5a supply voltage and increases less quickly: TS7107 starts to conduct. The collector current of TS7107 flows through R3105, causing the voltage on b-TS7108 to increase and TS7108 to conduct. Positive feedback is obtained via R3106 to drive TS7108 into conduction faster. When TS7108 is conducting, c-TS7108 is low just as pin 18 of IC7105. b-TS7106 goes low via R3103, so that TS7106 starts to conduct. Pin 17 goes high (RESET) via R3102.
As soon as the voltage on the slider of R3108 exceeds 2.7 V, TS7107 will cut off. The collector current of TS7107 decreases, the voltage across R3105 decreases and TS7108 cuts off. C-TS7108 goes high, b-TS7106 goes high and TS7106 cuts off. C2101 starts to charge via the internal pull-down resistor between pin 17 and ground inside the microcomputer. This causes the voltage at pin 17 to decrease. If the voltage across the capacitor is sufficiently high, the microcomputer will adopt the RUN state.

After switch-off or failure of the +5a supply voltage, C2102 can discharge across D6101.
D6101 also protects the reset input of the microcomputer against the negative voltage of electrolytic capacitor C2101 after switch-off or failure of the +5a supply voltage.

3.7.2 Voltage guard

The voltage guard of the +5a power supply is realized as follows: b-TS7107 is driven via voltage divider R3107, R3108 and R3110. This causes the voltage at b-TS7107 to follow the +5a supply voltage. If the voltage at b-TS7107 drops below 2.7 V, TS7107 will start to conduct. Consequently, TS7108 also starts to conduct, c-TS7108 goes low, TS7106 starts to conduct via R3103 and pin 17 goes high: RESET.
The reset value for the +5a supply voltage is adjustable with potentiometer R3108. The adjustment is as follows:
- Switch the TV into the teletext mode.
- Turn potentiometer R3108 fully anti-clockwise, considered from the component side.
- Connect a voltmeter or an oscilloscope between ground and pin 17 of IC7105 (RESET).
- Turn potentiometer R3108 slowly clockwise until the voltage at pin 17-IC7105 drops to a low level.

If the voltage protection is correctly adjusted, the circuit will reset the microcomputer when negative spikes occur on the +5a power supply.

3.7.3 Self-resetting

The microcomputer can reset itself by rendering pin 18 low.
As a result, a low level is applied via voltage divider R3103/ R31[illegible] b-TS7106, causing TS7106 to conduct. C3101 is dis[illegible]ed across TS7106, so that the voltage level at pin 17 [illegible]ses.
As s[illegible] as the voltage exceeds 2 V, the microcomputer will be reset. Self-resetting occurs in the following cases:
- At change-over from teletext mode to TV mode;
- When faults occur in transfers via the IIC bus;
- When software faults occu[illegible] the microcomputer, for example as a result of flash-over.

When the microcomputer is reset, that is when pin 17 is high, the system will not react to control commands relating to teletext.

If the set is in TV mode, and the microcomputer is reset, no change-over can take place from TV to TXT mode. If the set is in TXT mode, and the microcomputer is reset, it is not possible to select pages and to change over to TV mode.
The clock of teletext does run; the pages are also refreshed (VIP-CCT activity). In case of reset, there is no activity on the IIC bus.

4. THE CCT-IC

4.1 Introduction

The 40-pin CCT-IC is responsible for all digital functions relating to the processing of the teletext signal. The IC functions in co-operation with video input processor SAA5030 or SAA5230 and a page memory (static or pseudostatic RAM).
The CCT–IC is controlled by a microcomputer via the standard IIC bus.

4.2 Block diagram

The block diagram of the CCT-IC is shown in Fig. 4.1.
The five major functions of the IC are shown in the diagram as separate blocks:
1. Data Acquisition
2. Memory Interface
3. Character Generator
4. Timing Chain
5. IIC Interface and Control

The functional operation of the CCT-IC can be summarized as follows:
The data acquisition function is provided with serial teletext data and clock signals from the video input processor (VIP) via pins TTD and TTC. The data acquisition function converts the serial data into parallel form and then checks it for correctness on the basis of Hamming and parity checks. The Memory Interface arranges the communication between the CCT-IC and the external page memory. Using the eight parallel data inputs and outputs (D0 - D7) and the 13 address outputs (A0 - A12) a memory of maximum 8K x 8 bits (8 pages) can be controlled.
Writing to and reading from the memory takes place under control of the signals $\overline{OE}$ (output enable) and $\overline{WE}$ (write enable).
The checked data from the Data Acquisition function is written into the external page memory by the Memory Interface function.
The information stored in the page memory is applied via the Memory Interface to the character generator. The character generator translates the applied data into control signals for the TV. The output buffers R, G and B supply red, green and blue dot information, respectively. Blanking signals for the TV picture are supplied via the BLAN pin. The Y-output is active for the character foreground only, independent of colours, and does not contain the flashing function.

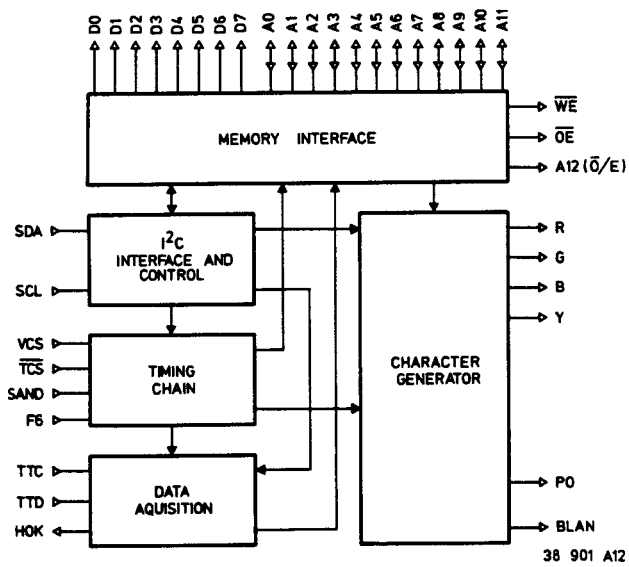


Fig. 4.1

Timing signals for the entire circuit are provided by the Timing Chain function which operates from the 6 MHz clock (F6) from VIP2.
The Timing Chain function also guards the signal quality. From the F6 signal the so-called SAND signal is generated, which is fed back as reference signal to the Phase Locked Oscillator in the videoprocessor for line synchronization of F6 with the incoming video signal. The composite sync signal VCS from VIP2 is used for frame synchronization of the CCT timing. The Timing Chain circuit generates a composite sync signal TCS which is used to drive the display time basis via VIP2. The TCS signal can be switched off under IIC bus control. As soon as this happens, VIP2 automatically provides composite video on the STTV (Sync To TV) pin for the synchronization of normal TV picture. The IIC Interface and Control section is responsible for the communication of the CCT-IC with the IIC bus (SCL and SDA lines). The variable functions of the CCT-IC are controlled via this bus. The CCT-IC operates from a single 5 V power supply.

In the following sections, the working of the various circuits is treated in more detail.

4.3 IIC Interface and CCT control

4.3.1 Format of IIC transfers

For the communication between microcomputer IC7105 and CCT IC7101 (see circuit diagram in Appendix C), use is made of a standard IIC bus. Resistors R3125 and R3126 are the pull-up resistors for the open-collector bus drivers of both ICs. If the bus is not used, both bus lines are high. This is the case, for example, during the reset state of the microcomputer. In Appendix A the basic procedures for transfers via this bus are given.

Since the CCT-IC is a so-called slave transceiver, the data clock (SCL) is always generated by the master, the microcomputer. This is true for both writing to and reading from the CCT-IC. Consequently, the SCL pin is only input.
The data transfer via the SDA line does take place bidirectionally, so that the SDA pin (20-IC7101) can be both input and open-drain output.

Only the microcomputer can start a data transfer via the IIC bus. A transfer always begins with a start condition (S) (see Fig. 4.2). The start condition is followed by the slave address that is used by the microcomputer to indicate that the IIC command is meant for the CCT-IC. The CCT slave address is fixed (mask programmed) at value 0010001.
The 7-bit slave address is followed by a single bit which indicates the direction of the data flow (reading or writing). If the bit is set to "reading", the data output buffer of the CCT-IC will be switched on so that data from the CCT-IC can be transferred to the bus. The processor can end the transfer by not giving an "acknowledge" on the last data byte.
If the bit is set to "writing", the data output buffer is switched on only to give an acknowledge on every data byte of the microcomputer.

A transfer involving writing to or reading from the CCT-IC generally contains, in addition to the slave address and the read/write bit, an 8-bit subaddress. This subaddress selects one of the eleven available registers (R1 to R11) inside the CCT-IC. All communication with the CCT-IC takes place via these registers. If a register has already been addressed in a previous transfer, the subaddress may be omitted in a following transfer.

The address is followed by the actual data. In principle, an unlimited number of databytes may be transmitted.
The receipt of each databyte must be confirmed by means of an "Acknowledge". The transfer of data is ended by a stop condition (P).

4.3.2 The CCT control registers

Figure 4.3 gives a survey of the control functions that are performed by the registers. The eleven registers can functionally be divided into three groups:

The first group, consisting of registers R1, R2 and R3, contains the mode of the decoder and the data for a requested page.
The second group, consisting of registers R4, R5, R6 and R7, contains data for the reproduction of a page.
The third group, consisting of registers R8, R9, R10 and R11, controls the external page memory.
A survey of the functions of the various registers is given in Appendix B.

The microcomputer can write information to all registers, but can only read from register R11. As register R11 corresponds directly to the page memory, only the contents of the page memory can be read and not the status of the control registers. If it is necessary that the status of a bit from a register is retained for software purposes, the microcomputer should do this itself.

All registers in the CCT-IC can be addressed directly via the IIC bus. This is possible because every register has its own subaddress. As the subaddress is defined as the second byte after the start condition, the IIC transfer must be stopped and restarted to transmit a new subaddress. As mode registers within **one** group are often set together, they can be filled in **one** IIC bus transfer, without extra stop and start conditions (this is the so-called auto Increment facility).

To request a page, registers R1 to R3 should be set (see figure 4.4.a). R1 is addressed by means of its subaddress. After a databyte has been written to R1, R2 is automatically adressed (auto increment facility). After a databyte has been written to R2, R3 is automatically addressed. Depending on the contents of R2, a maximum of seven databytes can be written to R3. Register R3 contains seven subregisters (columns), numbered C0 to C6, which are successively filled with the databytes written to R3, starting with the subregister that has been defined in R2.
After C6 of R3 has been filled, no new register is automatically addressed and therefore the data transfer should be ended. The IIC format of this transfer is shown in Fig. 4.4.1.

To display a requested page, registers R4 to R7 should be set.
These registers are filled by means of the auto increment facility in the same way as registers R1 to R3. Registers R4 to R7 do not contain subregisters and can only contain **one** byte each.
The transmission is shown in Fig. 4.4.b. Register R4 is addressed via its subaddress. The first databyte after this subaddress is stored in R4. The second databyte is automatically stored in R5, the third databyte in R6 and the fourth databyte in R7, unless the transmission is ended sooner by a stop condition. After the fourth databyte no further automatic addressing takes place, so that the transfer will have to be ended.

For reading or writing data to the page memory, registers R8 to R11 are used. These registers can also be set in one transmission with the auto increment facility. R8, R9 and R10 contain the address of a location in the external page memory, while the data are being read or written to this location via R11. The transmission is shown in Fig. 4.4c. R8 is addressed by means of its subaddress.

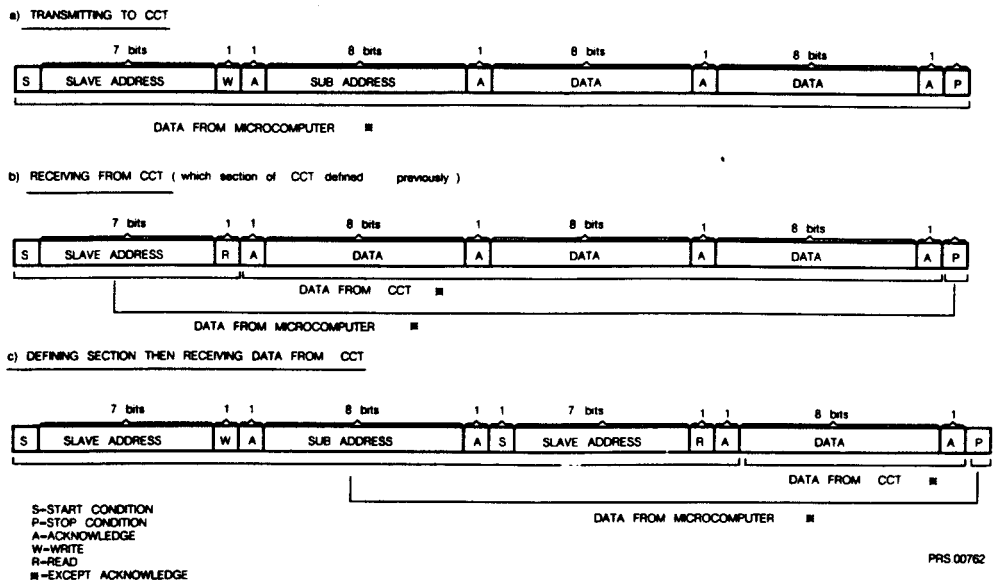


Fig. 4.2

Then the three following databytes are used to write a start address within the page memory in registers R8, R9 and R10. After the start address has been written to R10, R11 is addressed.
After each databyte that is now written to R11 and that is written in the memory location indicated by registers R8, R9 and R10, the contents of R8, R9 and R10 are automatically increased. This means that the next location in the external page memory is addressed.
In this way a series of characters can be written in the memory in **one** IIC transmission. See Fig. 4.4c.

To read data from the memory (via R11), registers R8, R9 and R10 should first be set to the correct start address by means of a write cycle. Then the direction of the data flow is reversed from writing to reading by generating a new start condition and by addressing the CCT IC with its slave address. The subaddress of R11 need not be transferred, because R11 remains addressed after the setting of (R8, R9 and) R10.

SUBREGISTER NO / REGISTER NO		REGISTER BITS D7	D6	D5	D4	D3	D2	D1	D0	REGISTER FUNCTIONS	
R1		TA	$\overline{7+8}$/ 8 BIT	ACQ $\overline{\text{ON/OFF}}$	GHOST ROW ENABLE	$\overline{\text{DEW}}$/ FULL CHANNEL	TCS ON	T1	T0	MODE CONTROL	
R2		—	BANK SELECT A2	ACQ. CCT A1	ACQ CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	PAGE REQUEST ADDRESS	↗
R3	C0	—	—	—	DO CARE	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0	PAGE REQUEST DATA (MAGAZINE)	↗
R3	C1	—	—	—	DO CARE	PT3	PT2	PT1	PT0	PAGE REQUEST DATA (PAGE TENS)	↗
R3	C2	—	—	—	DO CARE	PU3	PU2	PU1	PU0	PAGE REQUEST DATA (PAGE UNITS)	↗
R3	C3	—	—	—	DO CARE			HT1	HT0	PAGE REQUEST DATA (HOURS TENS)	↗
R3	C4	—	—	—	DO CARE	HU3	HU2	HU1	HU0	PAGE REQUEST DATA (HOURS UNITS)	↗
R3	C5	—	—	—	DO CARE		MT2	MT1	MT0	PAGE REQUEST DATA (MINUTES TENS)	↗
R3	C6	—	—	—	DO CARE	MU3	MU2	MU1	MU0	PAGE REQUEST DATA (MINUTES UNITS)	↗
R4		—	—	—	—	—	A2	A1	A0	DISPLAY CHAPTER	
R5		BK GND OUT	BK GND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	DISPLAY CONTROL NORMAL	↗
R6		BK GND OUT	BK GND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	DISPLAY CONTROL NEWSFLASH /SUBTITLE	↗
R7		STATUS ROW $\overline{\text{BTM/TOP}}$	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1–23	BOX ON 0	DISPLAY MODE	
R8		—	—	—	—	CLEAR MEMORY	A2	A1	A0	ACTIVE CHAPTER	
R9		—	—	—	R4	R3	R2	R1	R0	ACTIVE ROW	↗
R10		—	—	C5	C4	C3	C2	C1	C0	ACTIVE COLUMN	↗
R11		D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	ACTIVE DATA	

— Bit does not exist

↗ Auto increment

PRS.00761

Fig. 4.3

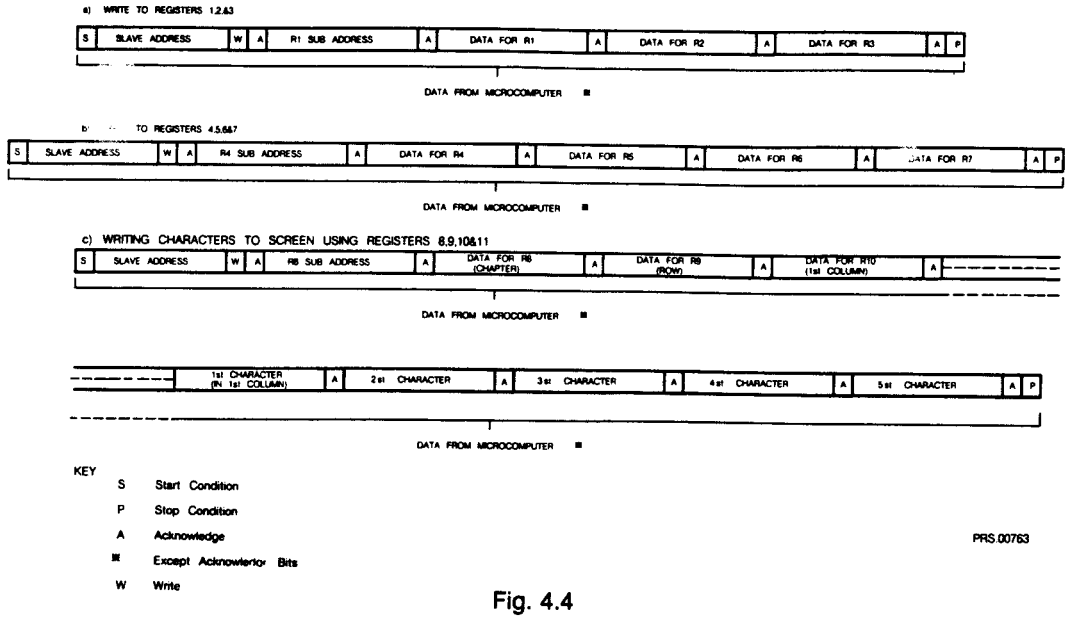


Fig. 4.4

EXAMPLE I^2C TRANSMISSION: REQUESTING PAGE 123 IN AQUISITION CIRCUIT NO.3 FOR MEMORY NO.3 (ASSUMES SUB-CODE DIGITS WERE NOT USED OR ARE UNALTERED)

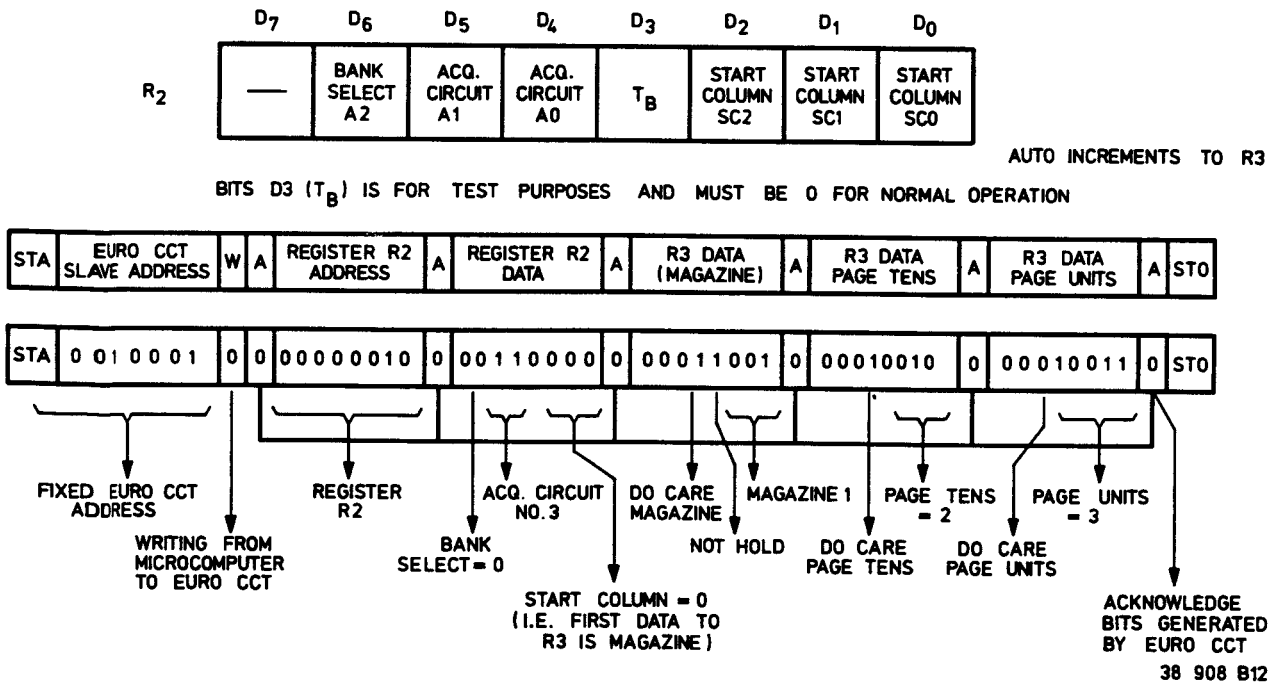

D7 D6 D5 D4 D3 D2 D1 D0
R2
—
BANK SELECT A2
ACQ. CIRCUIT A1
ACQ. CIRCUIT A0
TB
START COLUMN SC2
START COLUMN SC1
START COLUMN SC0
AUTO INCREMENTS TO R3
BITS D3 (TB) IS FOR TEST PURPOSES AND MUST BE 0 FOR NORMAL OPERATION
STA
EURO CCT SLAVE ADDRESS
W
A
REGISTER R2 ADDRESS
A
REGISTER R2 DATA
A
R3 DATA (MAGAZINE)
A
R3 DATA PAGE TENS
A
R3 DATA PAGE UNITS
A
STO
STA 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 0 0 1 1 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 1 1 0 STO
FIXED EURO CCT ADDRESS
WRITING FROM MICROCOMPUTER TO EURO CCT
REGISTER R2
BANK SELECT = 0
ACQ. CIRCUIT NO.3
START COLUMN = 0 (I.E. FIRST DATA TO R3 IS MAGAZINE)
DO CARE MAGAZINE
NOT HOLD
MAGAZINE 1
DO CARE PAGE TENS
PAGE TENS = 2
DO CARE PAGE UNITS
PAGE UNITS = 3
ACKNOWLEDGE BITS GENERATED BY EURO CCT
38 908 B12

Fig. 4.4d

When the TV is connected to an aerial signal without teletext information (for example a pattern generator), and the TV is in TXT mode, there will be a fixed pattern on the IIC bus. This pattern (Fig. 4.5) arranges the communication between the microcomputer and the CCT IC when pages P100 and P101 are being looked for. The pattern can be made visible on an oscilloscope with delayed time basis and has the following meaning: see Fig. 4.5.

START : High to low transition of the SDA line while SCL is high.

ADDRESS CCT : The address of the CCT-IC is mask programmed at 0010001.
The logic level of SDA is true when SCL is high.

WRITE : 8th bit of the first byte, the bit after the slave address, gives the direction of the datatransfer 1 = read 0 = write

ACKNOWLEDGE : Acknowledgement of receipt of a byte by the slave.
Acknowledge is a logic low level of SDA while SCL is high.

SUBADDRESS : Addressing of a register in the CCT IC. Here register R8 is addressed.

DATA R8 : Data for the register (R8) addressed with the subaddress. The contents of this register indicate the chapter inside the page memory. As this CCT decoder is equipped with two memory blocks (that is, storage facility for two teletext pages), the contents of R8 can either be "0" or "1".
After a byte has been written in R8, R9 is automatically addressed.

DATA R9 : The contents of R9 give the row number of the teletext page.
In this case row 25. After a byte has been written in R9, R10 is automatically addressed.

DATA R10 : The contents of R10 give a character column of a teletext page.
A row is built up of 40 character columns (character position inside a row). Here column 8 is addressed.
After a byte has been written in R10, R11 is automatically addressed.

RESTART : After addressing column 8 of row 25 in memory block 0 or 1, the CCT IC is set in the read position. This is done with a new start condition (high to low transition of SDA while SCL is high), the addressing of the CCT-IC (0010001) and by setting the read bit.

DATA R11 : Via register R11, which is addressed after the setting of R10, the contents of column 8, row 25, memory block 0 or 1 are read. The function contents of row 25 are shown in Fig. 4.6. Column 8 contains the $\overline{\text{FOUND}}$ bit which indicates if the requested page has been found. The microcomputer tests if the requested pages P100 and P101 have been found. Bit 5 in the IIC pattern (Fig. 4.5) indicates with a high level that the pages have not been found yet. The $\overline{\text{FOUND}}$ bit is high. Bit 6 is also high but has no meaning (don't care).

NO ACKNOWLEDGE : The master, the microcomputer, ends the data transfer from the CCT-IC by not giving an acknowledge to the CCT-IC.
The CCT-IC then stops the output of data.

STOP : The microcomputer (master) generates a stop condition with which the test cycle is ended.

START : After a waiting time the cycle is restarted with a high to low transition of the SDA line while SCL is high.

BIT \ COLUMN	0	1	2	3	4	5	6	7	8	9
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0

MAG MAGAZINE
PU PAGE UNITS
PT PAGE TENS
} PAGE NUMBER

MU MINUTES UNITS
MT MINUTES TENS
HU HOURS UNITS
HT HOURS TENS
} PAGE SUB-CODE

$\overline{\text{FOUND}}$ LOW FOR PAGE HAS BEEN FOUND
PBLF PAGE IS BEING LOOKED FOR
HAM.ER. HAMMING ERROR N CORRESPONDING BYTE

Fig. 4.6

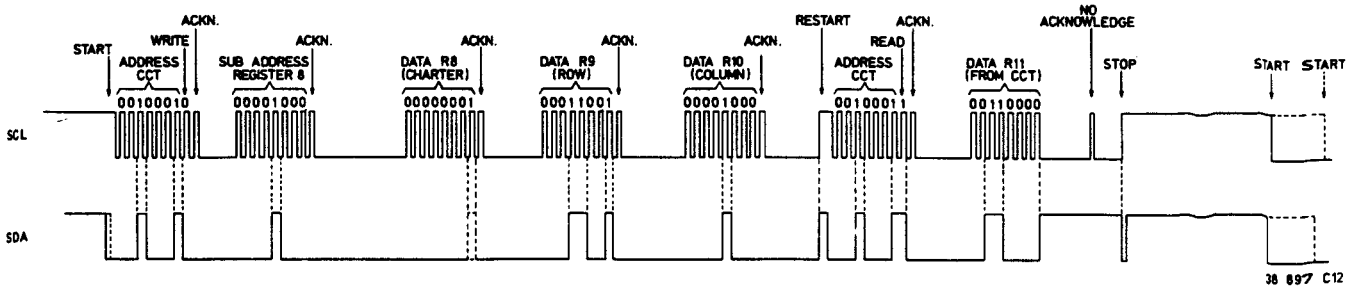


Fig. 4.5

4.4 Data Acquisition function

4.4.1 Data Acquisition Principles

The teletext information is transmitted according to the format shown in Fig. 4.7. Every teletext data line has two bytes in Hamming code which contain the magazine and row number of that data line. The magazine number indicates the page hundreds and can vary from 1 to 8. The row number gives the number of the row within the page and can vary from 0 to 31.
We can distinguish between three types of rows:

- Data rows which have row number 0 are page headers. Fig. 4.8 gives the structure of the page headers. The bits that are indicated with an "M" (message) contain the real data. The bits indicated with a "P" (protection) have been added for the Hamming-code. In addition to the two bytes of the magazine and row number, the page header contains 8 bytes in Hamming code. These bytes contain the page number (tens and units), the page sub-code, also called time code, and a few control bits. The remaining 32 bytes represent characters that are displayed on the screen. They contain a transmitter indication, the date and the page number. The last eight of these 32 characters are specially reserved for the time.

- Rows that have row number ... 23 contain the actual page information. Every r... ...ntains the information for 40 characters on the s... ...en. The structures of these rows are shown in Fig. 4.9.

- Rows which have row numbers 24 to 31 are ghost rows. They are called like that because they are not recognized by the first-generation decoders. The CCT-decoder is a decoder of the second generation and is capable of recognizing these ghost rows. These rows are used to transmit extra data and control information (see section 4.4.3).

The structure and function of the rows that can be received and processed by the CCT-IC are given in Fig. 4.10.

When a valid page header is received, the last eight characters are stored independent of the requested page. As a result the actual time is displayed at the top right. As long as a page is being looked for, the remaining 24 display characters of the page header are stored as well, producing the effect of the rotating page numbers. As soon as the page header of a requested page is received, the corresponding normal rows are stored.

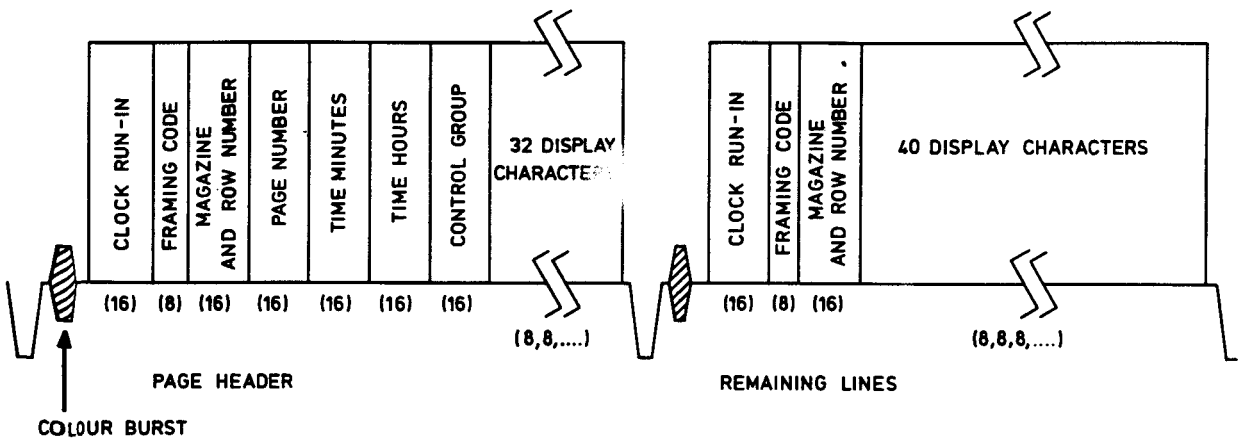
4.4.2 Requesting a page

Seven digits are used to identify a page: 3 digits for the page number (magazine, page tens, page units) and 4 digits for the sub-code (hours tens, hours units, minutes tens, minutes units). The denomination of the sub-code digits is derived from the sub-code's previous application as time page code.

This code was used to request a page at a time that was set in advance. This was possible because the actual time was filled in in the page header of each page in the sub-code bytes.

To look for a page, the page number and sub-code from the page headers received are compared with the values stated by the user, which are stored in register R3 (see section 4.3.2). The CCT-IC enables an arbitrary combination of these 7 digits to be involved in the comparison by (re)setting the do-care bits in R3. This option is only possible if provisions are made for it in the software of the microcomputer.
In the first-generation decoders a page can only be requested with a three-digit page number and possibly the four-digit sub-code.

For requesting normal teletext information, decimal digits are used for page number and sub-code. However, the CCT-IC can acquire pages in the entire hexadecimal range. The highest page number, if all available bits are "1", then is 7FF 3F7F$_{16}$ (2048 pages, 16255 subcodes). Hexadecimal page numbers can occur, for example, with transmissions from computer programmes via Teletext (telesoftware).



(THE FIGURES IN BRACKETS ARE THE NUMBER OF BINARY DIGITS)

35 869B12

Fig. 4.7

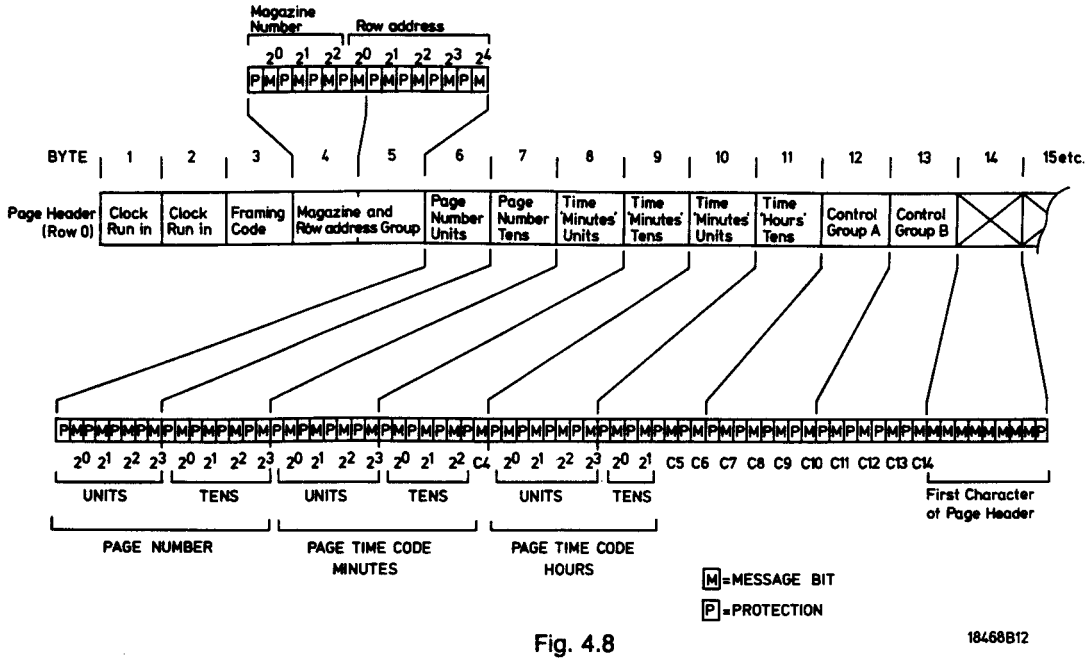


Fig. 4.8

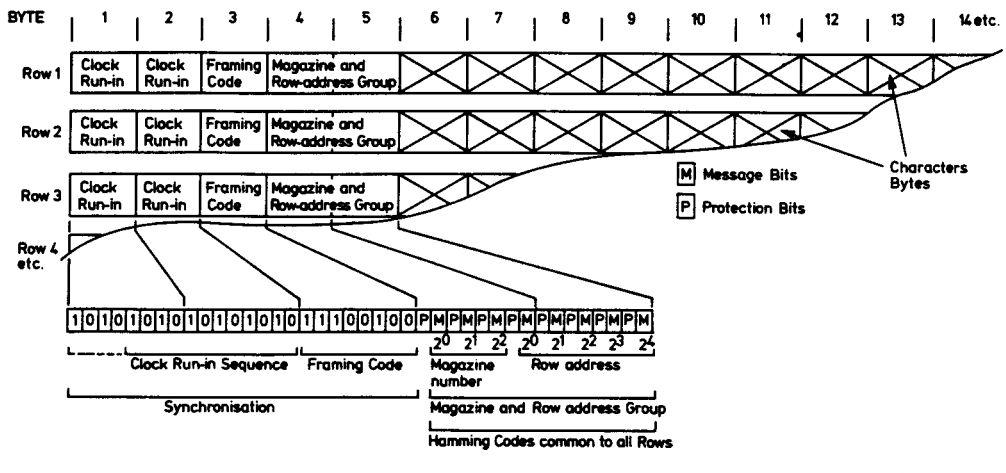


Fig. 4.9

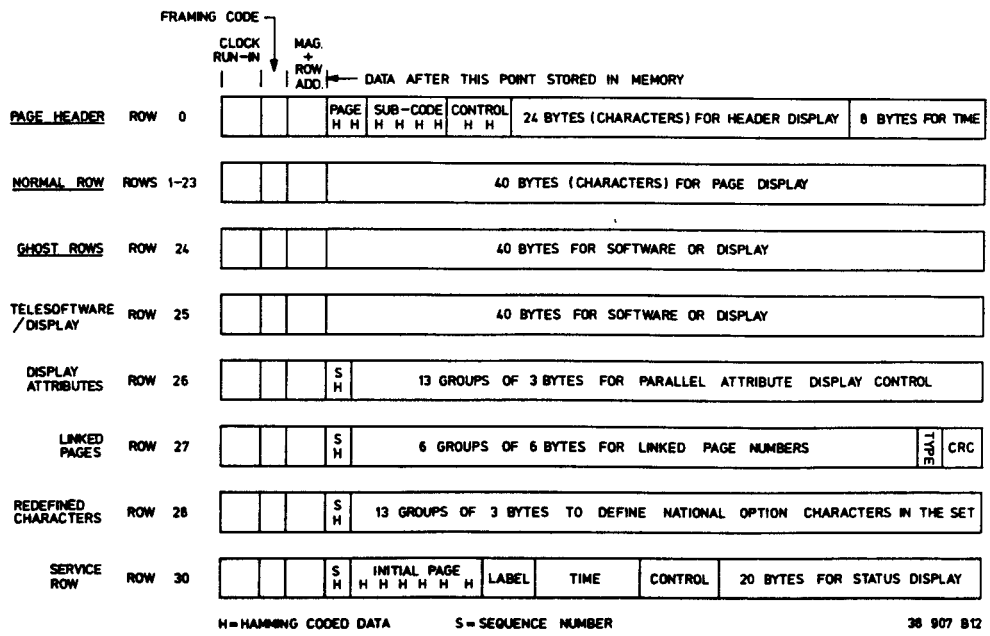

FRAMING CODE
CLOCK RUN-IN
MAG. + ROW ADD.
DATA AFTER THIS POINT STORED IN MEMORY
PAGE HEADER ROW 0
PAGE SUB-CODE CONTROL
24 BYTES (CHARACTERS) FOR HEADER DISPLAY
8 BYTES FOR TIME
NORMAL ROW ROWS 1-23
40 BYTES (CHARACTERS) FOR PAGE DISPLAY
GHOST ROWS ROW 24
40 BYTES FOR SOFTWARE OR DISPLAY
TELESOFTWARE / DISPLAY ROW 25
40 BYTES FOR SOFTWARE OR DISPLAY
DISPLAY ATTRIBUTES ROW 26
13 GROUPS OF 3 BYTES FOR PARALLEL ATTRIBUTE DISPLAY CONTROL
LINKED PAGES ROW 27
6 GROUPS OF 6 BYTES FOR LINKED PAGE NUMBERS
TYPE
CRC
REDEFINED CHARACTERS ROW 28
13 GROUPS OF 3 BYTES TO DEFINE NATIONAL OPTION CHARACTERS IN THE SET
SERVICE ROW ROW 30
INITIAL PAGE
LABEL
TIME
CONTROL
20 BYTES FOR STATUS DISPLAY
H=HAMMING CODED DATA
S=SEQUENCE NUMBER
38 907 B12

Fig. 4.10

4.4.3 Ghost Rows

Ghost Rows are extra rows, with row numbers 24 to 30, that are transmitted in addition to the normal teletext information. The ghost rows give extra display facilities. A survey is given in Fig. 4.11.
The CCT-IC is capable of receiving ghost rows and storing them in the page memory for further processing by the control microcomputer. This does not mean, however, that all ghost row possibilities can also be realized. In many cases the restrictive factors are the display facilities of the character generator function of the CCT–IC. For instance, pastel tints, double-width characters and special characters cannot be displayed by the character generator. With the aid of the CCT-IC and suitable ghost-row software it is possible to display several languages on one page, provided that the language-dependent characters lie within the set of 128 available characters.

In ghost row mode, a memory of 1K x 8 bits is used for the storage of normal page information (page header and text rows) and also 8 bits for the ghost row information. So, in ghost row mode, every page occupies 2K x 8 bits of memory.

Ghost rows 24 and 25 have the same format as normal rows and contain 40 characters. They may be used for extra display data, but also for transmission of computer programmes via teletext. Rows 24 and 25, in combination with rows 1 to 23 and the central 24 characters in row 0 (page header), form a page of 1024 bytes.
Ghost row 26 is used to enhance the display facilities.

15 rows (0 to 14) with ghost row 26 can be received by CCT when a sequence number is used after the row number. The data is transmitted in 13 groups of 3 bytes each. The first two bytes contain Hamming encoded address and mode descriptions whereas the third byte contains parity checked data.

The data from ghost row 26 can be read by the microcomputer and can then be used to overwrite the data from the normal rows. In this way, commands that cannot be transmitted via the normal teletext rows can be written into the page memory all the same (language-specific characters). The data from row 26 can also be used for the so-called parallel attributes which, just like the serial attributes in the normal teletext rows, indicate how a character should be interpreted, but now without space in case of a change of function (see section 4.6.4). Parallel attributes enable possibilities such as pastel colours, screen colours, row colours, accented and special characters double-height and double-width characters, underligned characters and characters with reduced intensity.
Although the CCT-IC can receive all these data, the character generator is not extensive enough to reproduce all these functions. In such a case, the CCT-IC is used for acquisitition while a suitable display circuit takes care of reproduction.

Ghost row 27 defines linked page addresses. Ghost row 27 contains 6 groups of 6 bytes, each of which specifies a page number and a subcode. There are four possible versions of ghost row 27, which are distinguished by means of a sequence number. In this way, a maximum of 24 page numbers can be linked with every stated received page.

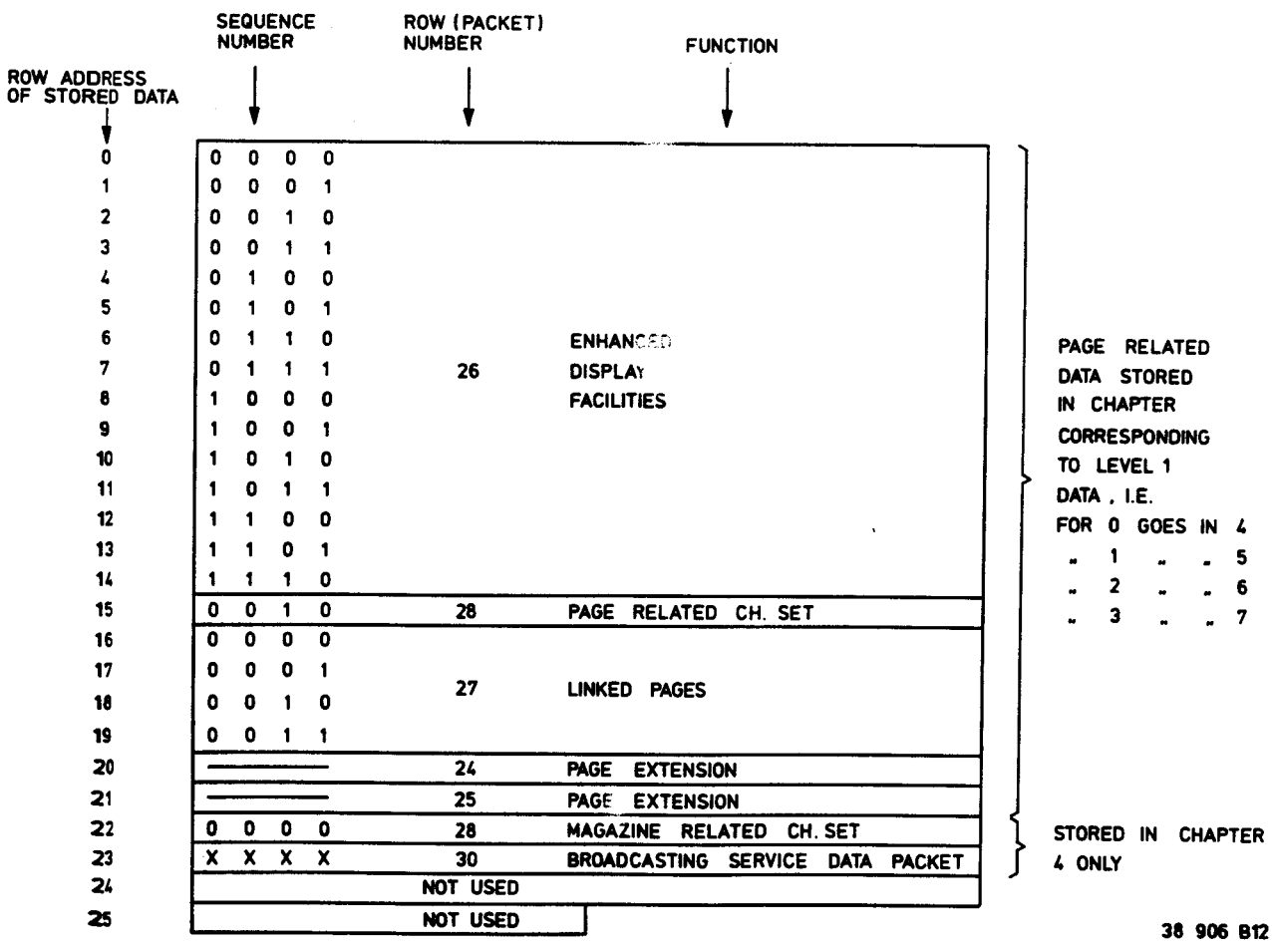


Fig. 4.11

The microcomputer reads the ghost row data and uses it in combination with user commands to determine which page should be looked for and displayed.
The CCT-IC can process all facilities of ghost row 27, provided that the microcomputer contains the supporting software to do this.

Ghost rows 28 are used to re-identify the character set. Two types are available: page related and magazine related ghost rows, both distinguished by a sequence number. The page related ghost row applies to **one** defined page, the magazine related ghost row applies to an entire magazine (group of pages having the same hundred in the page number). The data in ghost row 28 consists of 13 groups of 3 bytes each. Each group defines a character in the table of language specific characters. The magazine related ghost row is always stored in memory chapter 4, whereas the page related version is stored in the chapter that is related with the page received.
With the appropriate system software in the control microcomputer, the CCT-IC is able to process the ghost rows 28 in so far as this is permitted by the available character set.

Ghost row 30 gives general Information on the broadcasting and is called "Broadcasting Service Data Packet". This row is only transmitted in magazine 8 and applies to the entire broadcasting. When the row is received, it will always be stored in chapter 4. The sequence number is used to distinguish between data for field flyback mode and data for full channel mode (section 4.4.5). The microcomputer can read the sequence number and can switch over to the mode that is being used.
Ghost row 30 includes information on the first page that is looked for without intervention of the user, programme and channel labels, time control information and data for reproduction.
The possibilities of ghost row 30 can be processed by the CCT-IC when use is made of suitable system software.

4.4.4 Multipage Decoder

With a Multipage decoder more than óne page can simultaneously be looked for and stored in memory in óne transmission cycle. Of course, this requires extra memory space and a supporting programme in the control microcomputer.
The advantage of a Multipage Decoder is that the waiting time for searching new pages can be shortened. New pages can be looked for and stored in memory while a previously requested page is displayed on the screen. After reading the page on the screen, the user can immediately request one of the new pages from the memory.

The CCT-IC can look for, store and refresh 4 pages simultaneously. The circuit generally functions as if it consisted of 4 separate acquisition circuits: óne for every page.
The acquisition circuits can search for the pages using a preference list of page numbers (and sub-codes) stated by the user, or using data from ghost rows 27 with respect to linked pages.

4.4.5 Full Channel mode

In normal field flyback mode the CCT-IC only accepts data during lines 6 to 22 of each field. In full channel mode, data is accepted on all TV lines. In this mode, data transmission of 600 pages per second is possible, for example for use in cable TV networks.
In full channel mode it is not desirable that teletext data are multiplexed with a TV picture, because certain signal levels of the TV picture could be interpreted as teletext information, which could distort previously stored data.
Automatic change-over between field flyback and full channel mode can be obtained by means of the sequence number from ghost row 30. In this case, ghost row 30 should be transmitted during lines 6 to 22 to enable the decoder in field flyback mode to acquire the ghost row data.

The operation of the CCT-IC in full channel mode corrresponds largely to operation in normal field flyback mode. The only difference is that the old page cannot automatically be cleared anymore.
For, in field flyback mode, the rows are transmitted such that the page header and the normal rows of a page do not fall in the same field. Consequently, the display time of a TV picture is always available to clear the old page. In full channel mode, no time can be reserved for this, because it would considerably reduce the transmission capacity. In order to avoid mix-up with old data, all rows should be transmitted in full channel mode, also when they only contain spaces. As the new data always overwrites the old one, the old page need not separately be cleared in this situation.

4.4.6 Block diagram

The Data Acquisition section of the CCT-IC fulfils two main functions:
1. Acquiring the data (pages) desired by the user from the serial teletext signal TTD, which has been extracted from the video signal by the VIP2.
2. Generating control signals for the storage of the desired data in the page memories.

Figure 4.12 gives the block diagram.

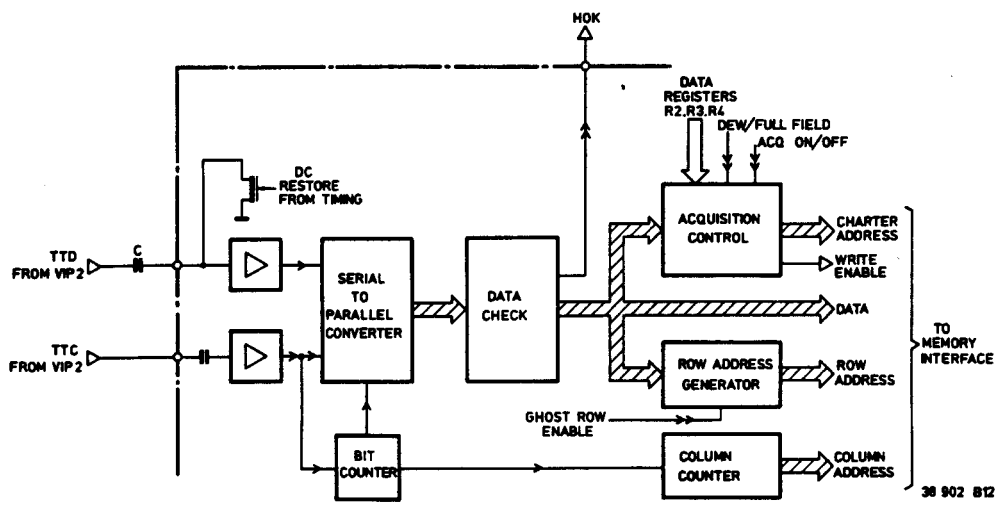


Fig. 4.12

The serial teletext signal TTD from the VIP2 is fed via an external coupling capacitor to the TTD pin of the CCT-IC. The TTD input is internally provided with a clamping transistor to ground, which is switched on from 4 µs to 8 µs of each line period. During this period, the input is kept at a low level (zero), causing the DC restore of the CCT input. Clock TTC is used to clock teletext data in the serial to parallel converter of the acquisition circuit. The clock has a frequency of 6.9375 MHz and is permanently available. The leading edges of the clock fall in the middle of the valid data period of the TTD signal.
The clock is fed directly from the VIP2 and is capacitance coupled in the CCT-IC to change the DC level.

In the serial-to-parallel converter block, the TTD signal is converted into parallel data words of 8 bits each. The moment from which groups of 8 bits are formed is determined by the so-called framing code, which is transmitted at the beginning of every teletext line (see Fig. 4.7). This goes as follows:
The incoming data is shifted in an 8-bit shift register by means of the TTC clock. At the same time, the contents of the shift register are compared with code 11100100, the correct value of the framing code. As soon as the contents of the shift register equal the reference code, the incoming serial data can be combined into groups of 8 bits (bytes). The bits are counted by the bit counter. The column counter then counts the bytes (characters) and, on the basis thereof, supplies column addresses to the memory interface for the storage of characters in the page memory.

In the Data Check circuit, the eight-bit data words are checked for transmission errors by means of Hamming and Parity checks. The magazine and row number of each teletext line and several bytes in the page header are transmitted in an error-correcting Hamming code.
With this code it is possible to detect and correct one erroneous bit and to detect several erroneous bits, and to refuse the row in that case. The data bytes are only provided with a parity bit. This parity bit can be removed, so that 7-bit data words are left over.
The Data Check circuit produces the control signal "HOK". This signal is a "flag" which indicates for each line whether a valid teletext signal has been received or not. The criterion for this is that all eight bits of the framing code are correct and that the first two hamming bytes (magazine and row numbers) do not contain any incorrigible errors. HOK stands for Hamming bytes O.K.. If the data is valid, the HOK signal will go high between 18 and 23 µs after the start of a line and will remain high until 7 µs after the start of the next line. If the data is invalid, the signal remains low. The HOK signal can be used to control an echo equaliser. If the signal is not used, the HOK pin may stay open.

The row number from the received teletext line is extracted from the checked data by the Row Address Generator and is then passed on to the Memory Interface function. The Row Address Generator can adapt its counting range if the reception of Ghost Rows is desired. In addition to their row number, Ghost Rows can also contain a sequence number which must be taken into account when storing the data in the memory. The Ghost Row mode is switched on under the influence of the Ghost Row enable bit (Register 1, bit 5).

The Acquisition Control Circuit sees to it that the pages requested by the user are extracted from the received teletext information. This is done by comparing the desired page numbers, which are written in register R3 after the IIC bus, with the received and checked information from the Data Check circuit.

Four pages can be requested can looked for simultaneously. The memory section where the page found must be stored is indicated by the Chapter Address.
The page memory consists of 8 chapters at the most. In a chapter the data for one teletext page (1024 bytes/characters) can be stored. The 8 chapters are divided among two memory banks, see Fig. 4.13.

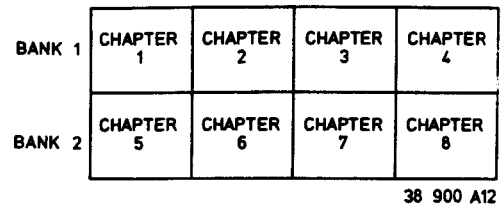


Fig. 4.13

In normal mode, chapters 1 to 4 from bank 1 or chapters 5 to 8 from bank 2 are simultaneously used for the storage and updating of the four pages that can simultaneously be searched for.
The change-over between bank 1 and bank 2 is dependent on the logic value of the Bank Select Bit (Register R2, bit D6). In Ghost Row mode the Bank Select Bit does not have any influence. The normal page information is written into chapter 1, 2, 3 or 4 and the corresponding ghost row data in chapter 5, 6, 7 and 8, respectively.

4.4.7 Stored data

Every page that is acquired by the acquisition circuit not only contains the characters that are displayed on the screen, but it also contains control and address information. All this information is stored in memory by means of the addresses supplied to the memory interface by the acquisition function. The memory division within a page (chapter) is given in Fig. 4.15.
A memory page is divided into 26 rows (row 0 to 25), rows 0 to 24 of which are displayed on the screen. The first seven bytes of row 0 can be filled by the microcomputer with status information, for example with the requested page number. The eighth byte is filled by the CCT hardware with the control character "alphanumerics white" or "alphanumerics green". With these control characters the colour of the next text will be displayed in green when the requested page is being searched for, and in white when the requested page has been found. The next 24 bytes in row 0 are filled with the 24 text characters from the page headers received. The last eight bytes are used for the actual clock time, also from the page headers received. Rows 1 to 23 contain the information of the normal teletext rows of the page, whereas row 24 contains the information of the so-called status row that is displayed above or below the main text.
The status row indicates in which status the decoder finds itself. In the status row, which is generated by the microcomputer, symbols indicate which teletext functions have been switched on by the user (double height, stop, acquisition, etc.). In Fig. 4.14 a survey of symbols and teletext functions is shown. The teletext symbol is used to indicate that the Teletext mode is switched on. This symbol has the same meaning as the Teletext LED on the front of TVs which have first-generation decoders. The status row furthermore gives the number of the page that is displayed on the screen and the numbers of the pages that are stored in the background memories.

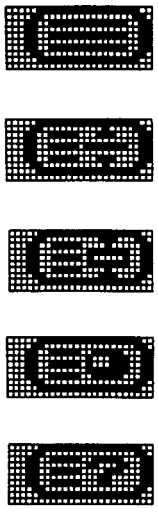
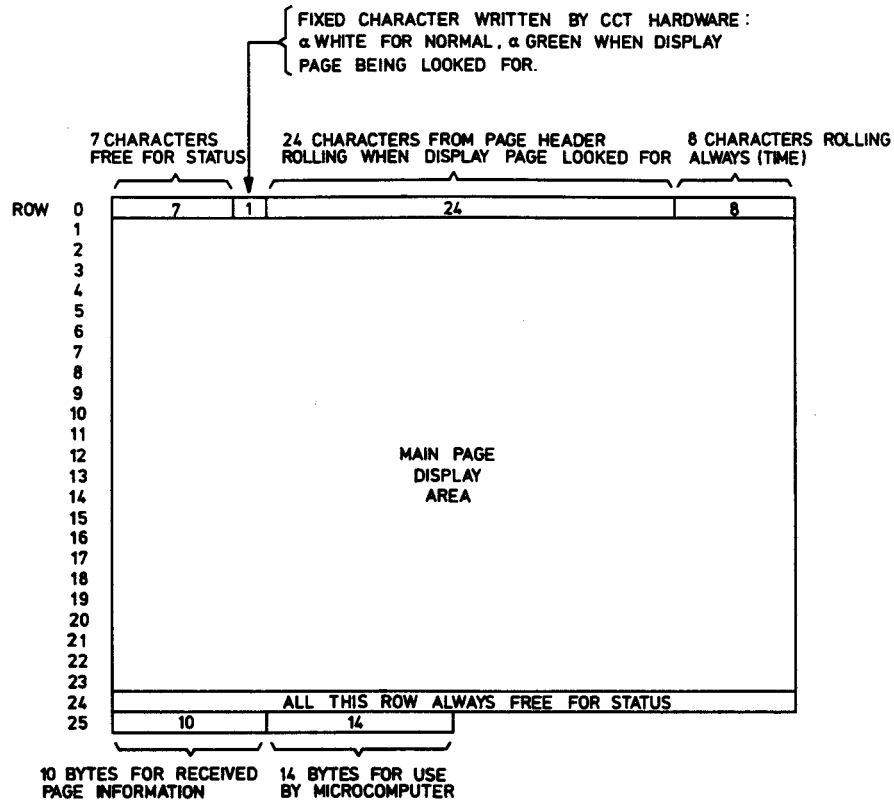


Fig. 4.14

The control and address information of the page is stored in row 25. This row is not displayed on the screen, but can be read via the IIC bus. Of the 24 bytes that are available in row 25, the first 10 are used for the storage of the page information received from the page header. The remaining 14 bytes are available for use by the microcomputer as normal RAM for general purposes.

The data contents of the first 10 bytes of row 25 are given in Fig. 4.15. Most bytes contain four information bits and a corresponding Hamming error flag. This flag will be set to "1" when an incorrigible multiple error is found in the four information bits. The flags can be used by the control software to take action in case of invalid data.
Row 25 contains, in addition to the page number and the page sub-code, the control bits from the page header (C4 to C14) and the page status bits FOUND and PBLF (Page Being Looked For). The treatment of these bits depends on their function. A survey of control bits C4 to C14 is given in section 4.6.6.



COLUMN / BIT	0	1	2	3	4	5	6	7	8	9
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	MAG3	0
D4	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	HAM.ER.	FOUND	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0

THE ABBREVIATIONS ARE :

MAG	MAGAZINE	PAGE NUMBER
PU	PAGE UNITS	
PT	PAGE TENS	
MU	MINUTES UNITS	PAGE SUB-CODE
MT	MINUTES TENS	
HU	HOURS UNITS	
HT	HOURS TENS	

PBLF PAGE IS BEING LOOKED FOR
HAM.ER. HAMMING ERROR IN CORRESPONDING BYTE
FOUND LOW FOR PAGE HAS BEEN FOUND

38 905 B12

Fig. 4.15

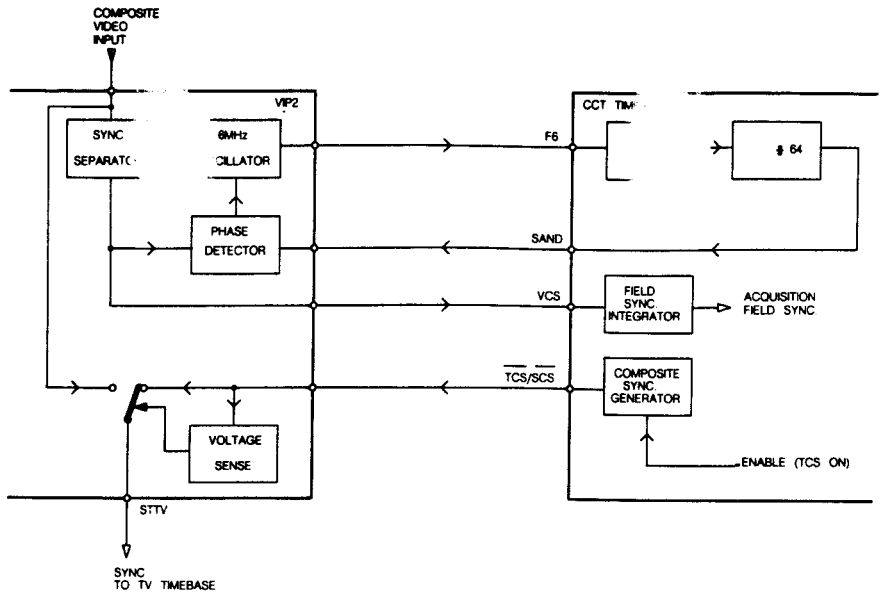


Fig. 4.16

PRS.00764

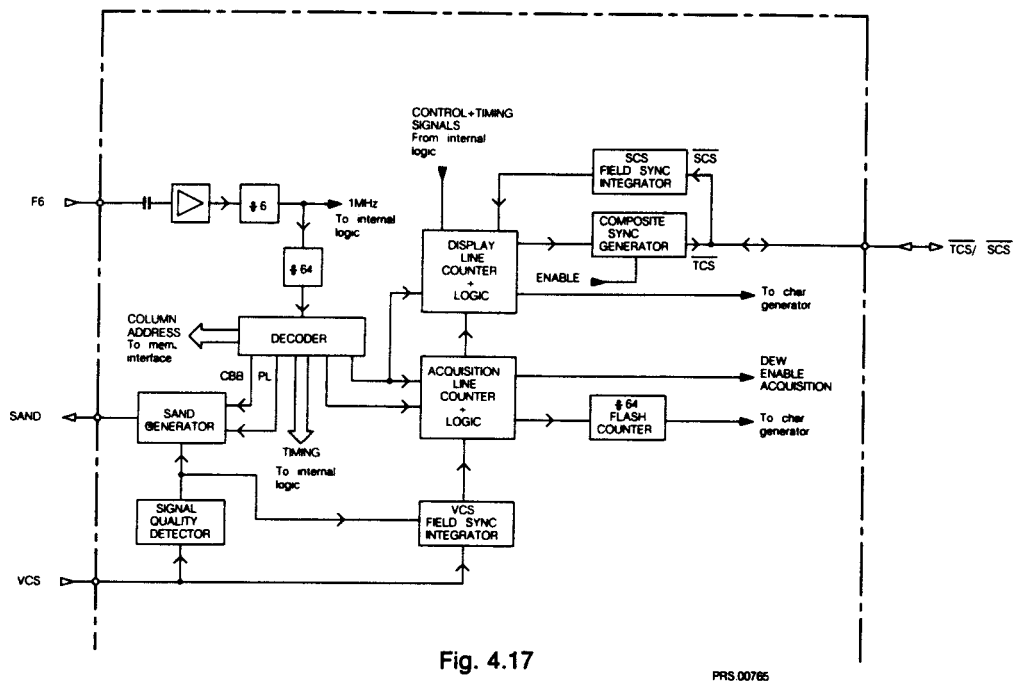


Fig. 4.17

PRS.00765

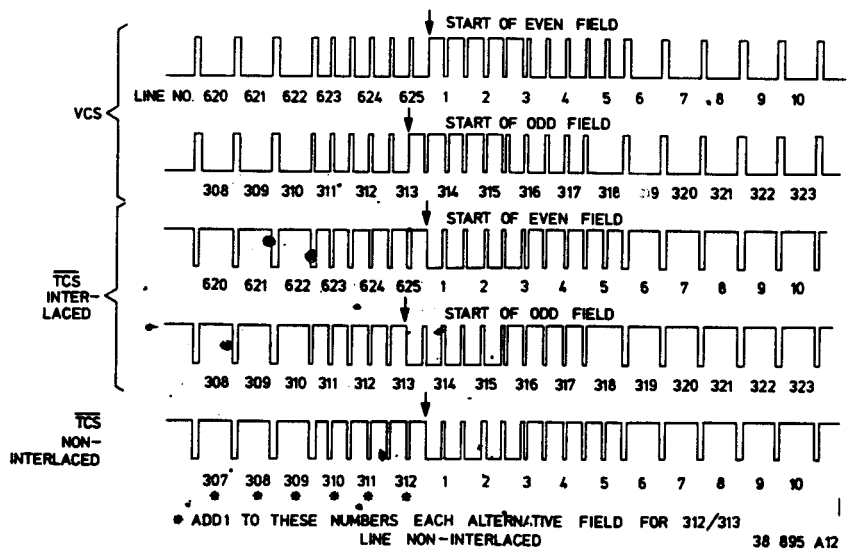


Fig. 4.18

4.5 Timing Chain Function

The timing chain function supplies timing signals to the various circuits in the CCT-IC and to the VIP2. The function furthermore guards the quality of the received teletext data by means of the digital signal quality detector.
In Figure 4.16 the connections between VIP2 and the timing chain section of the CCT-IC are shown. The block diagram of the timing chain function is given in Fig. 4.17.
The 6 MHz clock from VIP2 is fed to the F6 input. The signal is AC coupled, buffered and then divided by six to produce a 1 MHz clock. This is 1 MHz clock serves as a time basis for the circuits in the IC. Further division of the 1 MHz clock by 64 produces a line-frequent clock (15625 Hz) that is converted by a decoder in a number of line-frequent control signals. Two of these signals, CBB and PL, are fed to the SAND generator ciruit. The other signals are used for the delivery of count pulses to the acquisition and display line counter. The SAND generator circuit generates the three-level SAND signal. This signal is fed back to the video input processor as reference for the phase-locking of the F6 clock on the line synchronization of the incoming video signal. All line frequent timing signals in the CCT are thus phase-locked with the TV signal.

Field synchronization of the CCT-IC is realized by means of the composite sync signal, VCS, which is provided by the video input processor. The VCS signal also serves as information source for the digital signal quality detector.

In the VCS field sync integrator circuit, the VCS signal is integrated to remove interference peaks. Signals with noise can thus be processed in a more reliable way.
The integrating function of the VCS field sync integrator is obtained by digital process. The field sync integrator contains an up/down-counter which scans the logic level of VCS every microsecond.
The counter is increased if VCS is high and decreased if VCS is low. The counter position cannot become negative. When a specific (positive) counter position is reached, a field sync output pulse is provided. This counter position can only be reached during the wide equalizing pulses at the beginning of the field. The field output pulse is supplied at about $^3/_4$ of the line, after the start of the first field pulse.

The field sync integrator passes field sync pulses to the Acquisition Line Counter and Control block. After a field sync pulse is received by this block, further pulses are generated for at least 309 line periods. In this way a degree of protection is obtained against short interferences which otherwise could disturb the field synchronization and hence the capture of data.

If a field sync pulse is absent, the acquisition timing adopts the free-running mode, in which the original phase is maintained until a valid field sync pulse is received.

If the signal contains very much noise, the signal quality detector cuts off the field sync signal. Consequently the timing chain adopts the free running mode so that it can no longer be disturbed by noise signals from the field sync integrator.

The signal quality detector function is carried out in digital manner by the CCT-IC and not by the Video Input Processor as is the case with the TIC TAC TROM decoder. As soon as a signal with very much noise is fed to the teletext decoder, two undesired effects may occur. In the first place, the 6 MHz display clock generator in the VIP may have difficulties with synchronizing, which leads to unstable display of text on the screen. In the second place, the noise in the video signal may be interpreted by the acquisition circuit as valid teletext data, causing erroneous information to be written into memory and previously received pages to be distorted. These two problems can be solved by means of the signal quality detector. If a poor or absent signal is detected, the detector will switch the display clock (F6) in free-running mode and the display clock will cut off the data to the acquisition circuit.
The signal quality detection is done on the basis of the number of pulses in the VCS signal per line period. An undisturbed VCS signal contains óne pulse (line synchronization) or two pulses (equalization) per line. If the amount of noise in the signal increases, extra interference pulses will be introduced in the VCS signal. The criterion for detecting a poor line is that the line contains 3 or more pulses. When several poor lines have been detected, the data flow to the acquisition circuit will be stopped. Furthermore, the VCS signal will be blocked and the PL component will be removed from the SAND signal. This causes the F6 signal to be switched in free-running mode.

The Composite Sync Generator provides composite sync signals for the control of the display-time basis of the TV (see Fig. 4.18).
The so-called Text Composite Sync signal (TCS) is generated in conformity with the selected timing mode. This timing mode may be 312/313 lines interlaced, 312/313 lines or 312/312 lines non-interlaced.
The circuit generates line sync pulses until an initialisation signal is received from the acquisition or line counter. Then the equalization pulses are generated for $7^1/_2$ lines, followed again by line sync pulses. The composite sync generator is an independent circuit which is not dependent on the line counters. Once it is initiated, it produces the field synchronization series without intermission, thus avoiding synchronization disturbances.
The TCS signal is available on the $\overline{\text{TCS}}/\overline{\text{SCS}}$ pin. For field synchronization of the display timing this pin can also be used as input for an external composite sync signal $\underline{\text{SCS}}$ ($\underline{\text{Scan}}$ Composite Sync). In the teletext decoder, the $\overline{\text{TCS}}/\overline{\text{SCS}}$ pin is not used as input.

The last part of the timing chain function consists of a counter (divider-by-32) which provides the on/off signal for flashing characters. The circuit provides a signal with a period time of 1,28 sec. and a duty-cycle of 75%.

4.6 Character Generator Function

4.6.1 *Introduction*

The character generator function converts the teletext information that is stored in the page memory in video control signals for the TV receiver. The character generator function can generate 128 alphanumeric and 64 graphic (mosaic) characters. 32 control characters can determine the nature of the picture, such as the colour of the characters, the colour of the background, the height of the text and flashing. The characters are built up in a character matrix of 12x10 partitions (see Fig. 4.19). The block diagram is shown in Fig. 4.20.

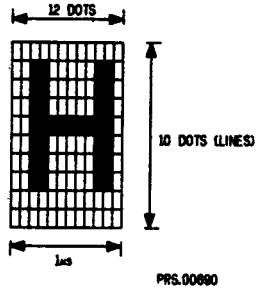


Fig. 4.19

The data from the page memory are fed to the character generator via the Memory Interface function. The data needed to display a teletext page on the screen can be divided into two main groups:

1. The character codes of the test to be displayed.
2. The page attributes of the page to be displayed.

A character code may indicate an alphanumeric character, a graphic sign or a control function. The codes are processed in the character address decoding, the graphics generator and the control character decoder circuits, respectively. See Fig. 4.20.

The page attributes contain the control bits from the page header of the page. In the first-generation decoders those data were processed directly.

As the CCT decoder can store several pages (multipage decoder), the data should be stored with the page, so that the page attributes change when another page is selected from the memory. When a page is displayed, its page attributes are stored in the page attribute latches.

4.6.2 *Formation of alphanumeric characters*

Character codes which relate to alphanumeric characters are converted by the character address decoding circuit and the ROM circuit into the dot pattern of the relevant character inside a matrix (see Fig. 4.19) of 12 dots horizontally and 10 dots vertically. The ROM has the information of the matrices of the 128 alphanumeric characters that can be displayed by the CCT-IC. A location inside the ROM is addressed with a column and a row address. Each alphanumeric character code is converted to a column address in the ROM by the character address decoding circuit. Here the language selection bits are taken into account.

The row addresses are provided by the line counter circuit, which indicates by 1 to 10 which line should be displayed. The contents of the addressed memory location appear at the output of the ROM: the dot pattern of the relevant character for one of the 10 matrix lines. This dot pattern is converted into serial information in the parallel to serial converter and is fed outside via the output logic.

Not all of the dots in the 12x10 matrix are used for the formation of alphanumeric characters. With most of the characters the top line of the matrix is left blank, so that boxed text or text having a different background colour is separated from the characters in the line above. The top line is sometimes used for displaying the accents above some characters.

The two bottom lines are only used for the tails of characters such as p or g. In horizontal direction the characters are usually separated by 2 dots on the left-hand side and 1 dot on the right-hand side of the matrix. The characters and digits from the character sets of both versions of the CCT-IC are shown in Figs. 4.21, 4.22 and 4.23.

4.6.3 *Formation of graphic characters*

Codes for graphic characters are not stored in a ROM, but are directly converted by the graphics generator into the block pattern for the relevant character. Graphic characters are formed in the character matrix from a pattern of 2x3 fields (Fig. 4.24a).

The bits b1 to b5 and b7 of the character code each represent one sixth of the graphic sign: the part for which the bit is "1" lights up. Bit b6 is always "1" for graphic characters.

Graphic characters can be displayed in two forms: in contiguous fields and in separated fields. See Fig. 4.24b/c.

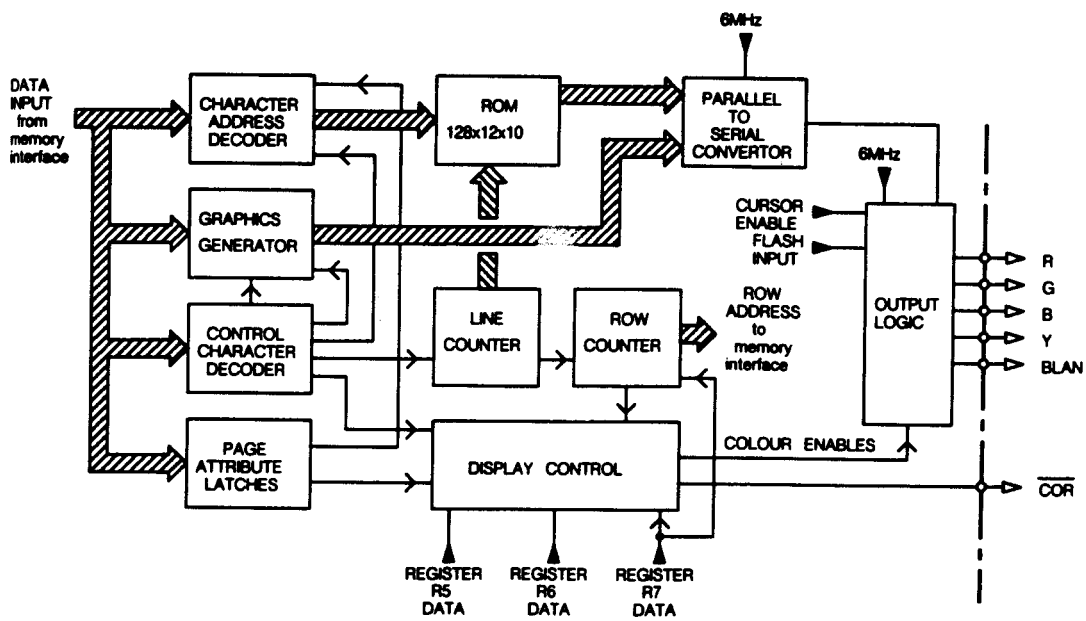


Fig. 4.20

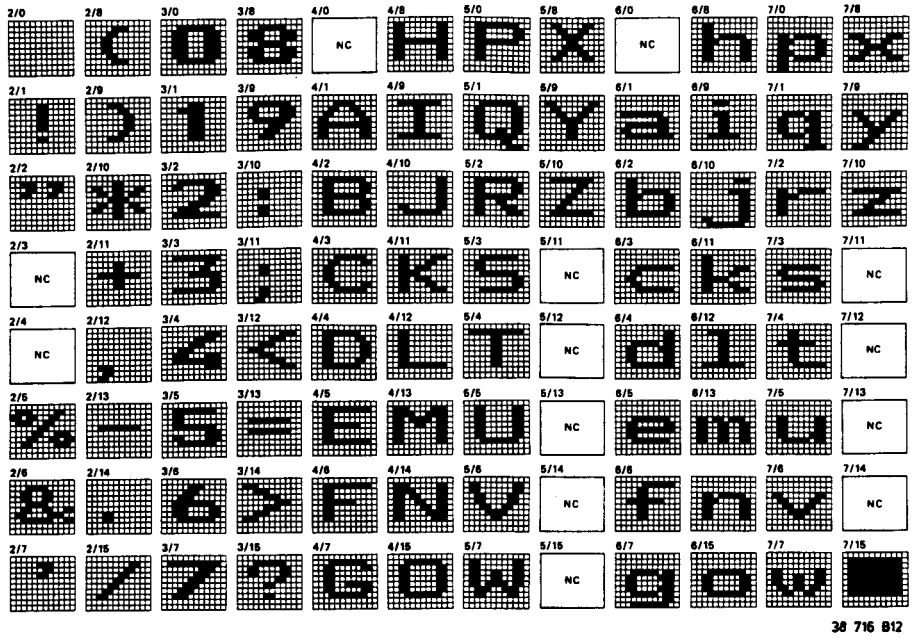


Fig. 4.21

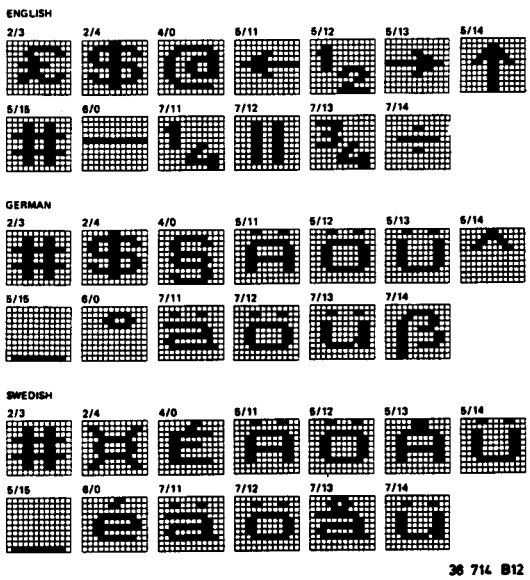


Fig. 4.22

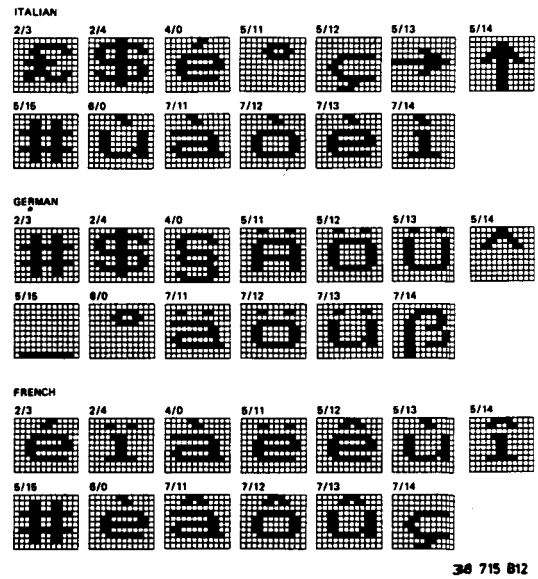


Fig. 4.23

DISPLAY OF GRAFICS

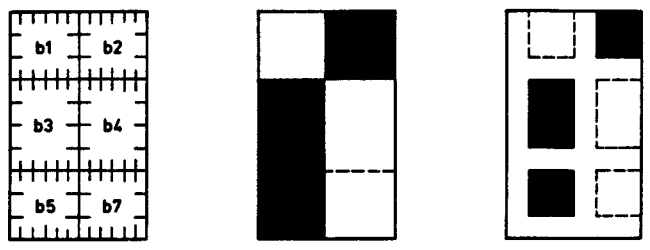


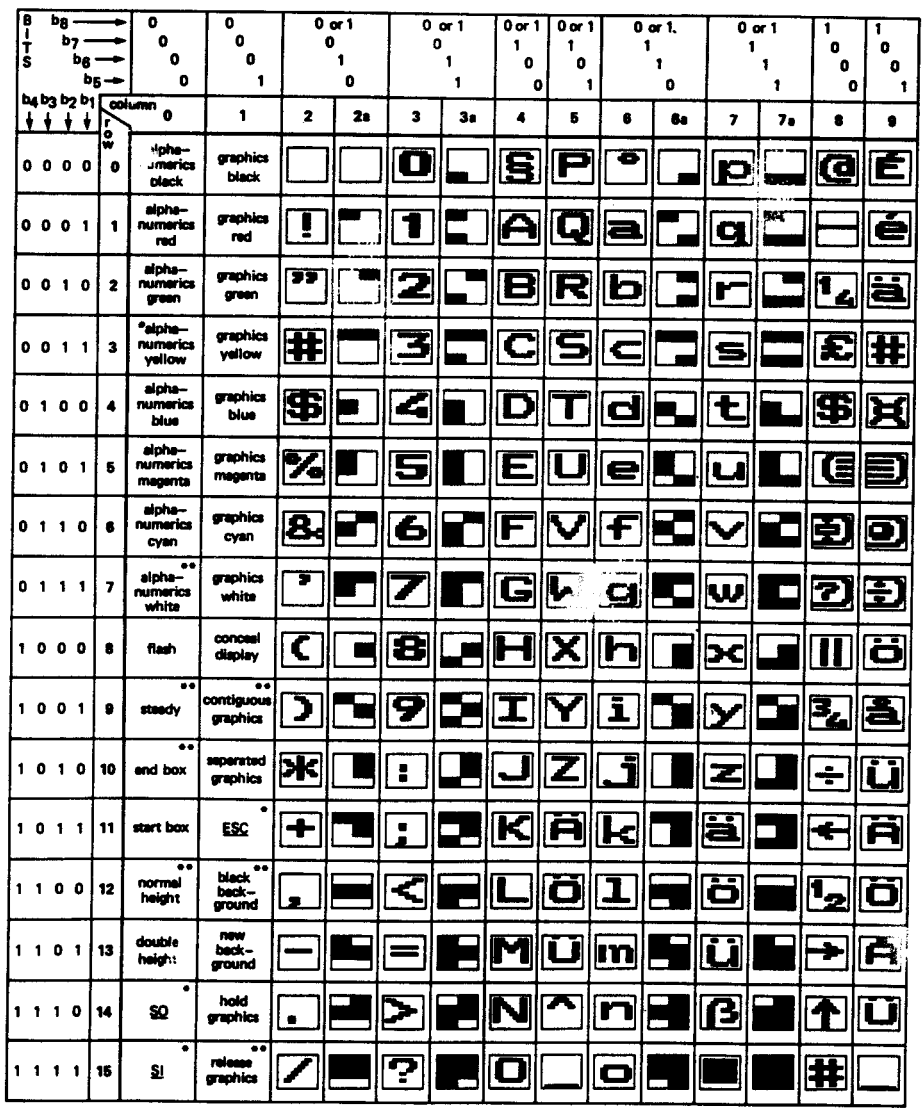
Fig. 4.24

4.6.4 *Control characters*

The control characters are decoded in the control character decoder and are used to increase the display facilities of the teletext. The teletext decoder is controlled with 7-bit codes with which a maximum of 128 (2^7) combinations can be formed. However, this number is too small to code the alphanumeric and the desired graphic characters (inclusive of colour, flashing of text, magnified display, etc.).
For this reason, teletext uses so-called serial attributes of control characters, in which 96 out of 128 possibilities are used for information and the remaining 32 for control. The control characters are transmitted **before** the information characters and indicate how the latter characters should be interpreted: as alphanumeric character or as graphic sign, what the colour is, etc.
Control characters are displayed on the screen as spaces. The space can be given the background colour of the preceding character. Several control characters can be given in succession.
The control character decoder circuit controls the Character Address Decoder and the Graphics Generator to distinguish between alphanumeric and graphic characters and to select the graphic possibilities (hold-release graphics, contiguous-separated graphics). The circuit also controls the line counters for double-height text display and the display control circuits for colour selection of the characters, boxing of text and flashing of characters. In addition to all display facilities of the TROM from the first-generation decoders, the CCT-IC also contains the facility to generate black characters and graphic signs on a coloured background. This is possible because of the addition of the control characters "alphanumerics black" (0/0) and "graphics black" (1/0).
Figures 4.25 and 4.26 give a survey of the total character sets, including the language specific characters and the status characters of CCT-ICs SAA5240A and SAA5240B.

4.6.5 *Language selection facilities*

The CCT-IC has the facility to display text in various languages, using characters that are specific to a given language area. All characters are stored in the ROM; they are addressed with 8-bit data words from the page memory. Bits 1 to 7 of these data words correspond with the 7-bit TXT codes that are transferred by the broadcasting, whereas bit 8 is filled in under microcomputer control. The data words from the page memory cannot readily be measured on data lines D0 to D7.
There are two methods of addressing the desired characters. Change-over between these two methods is done with bit 8 of the data words from the memory.


BITS b8 b7 b6 b5
b4 b3 b2 b1
column
row
0
1
2
2a
3
3a
4
5
6
6a
7
7a
8
9
0 0 0 0 0 alpha-numerics black graphics black
0 0 0 1 1 alpha-numerics red graphics red
0 0 1 0 2 alpha-numerics green graphics green
0 0 1 1 3 *alpha-numerics yellow graphics yellow
0 1 0 0 4 alpha-numerics blue graphics blue
0 1 0 1 5 alpha-numerics magenta graphics magenta
0 1 1 0 6 alpha-numerics cyan graphics cyan
0 1 1 1 7 alpha-numerics white graphics white
1 0 0 0 8 flash conceal display
1 0 0 1 9 steady contiguous graphics
1 0 1 0 10 end box separated graphics
1 0 1 1 11 start box ESC
1 1 0 0 12 normal height black background
1 1 0 1 13 double height new background
1 1 1 0 14 SO hold graphics
1 1 1 1 15 SI release graphics

* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

38 712 B12

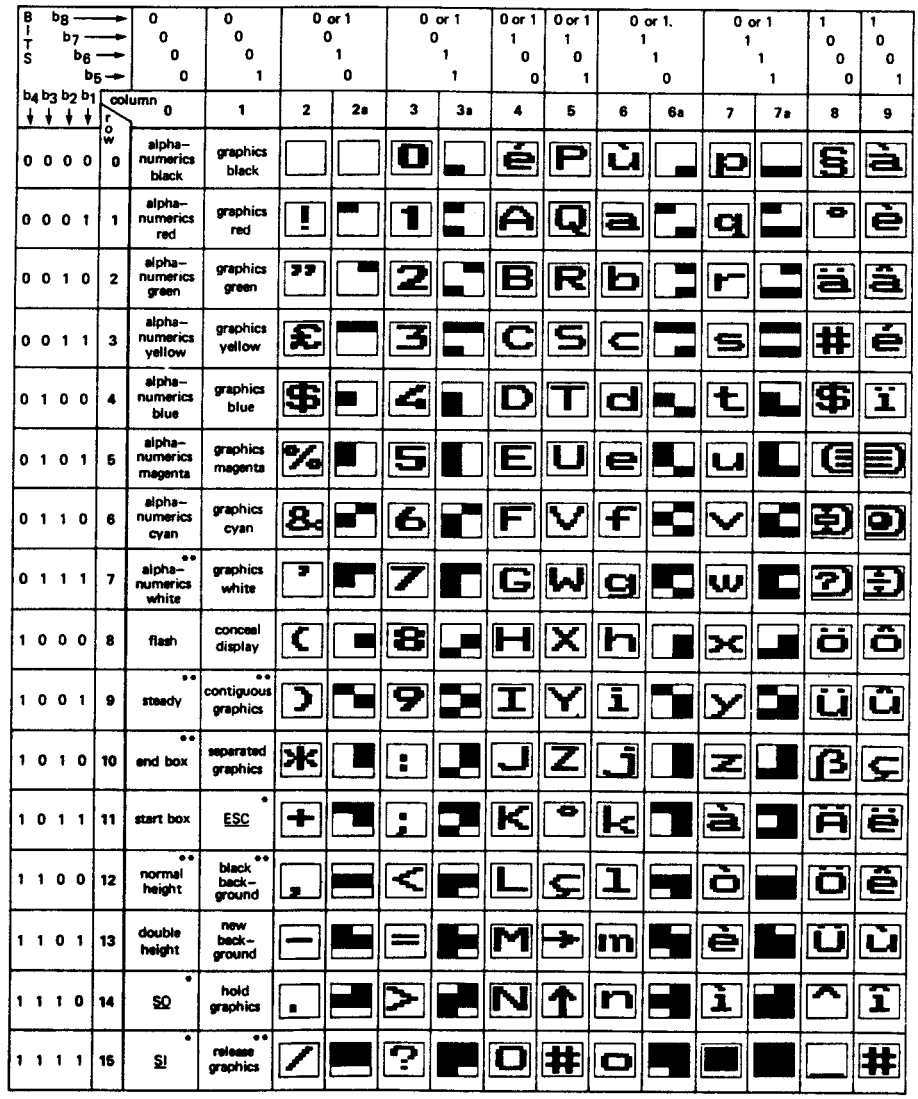
Fig. 4.25

The first method corresponds to that of level 1 teletext, where only óne language per page can be displayed. Language selection is realized with control bits C12, C13 and C14 from the page header of the page. Bit 8 of the data words from the memory is always zero with this method. With the remaining 7 bits a maximum of 96 display characters and 32 control characters can be addressed. 13 of the 96 display characters are changeable/replaceable for the various languages. This means that the language specific characters from one of the three tables with language specific characters that a CCT-IC can contain are filled in at the addresses of these 13 characters. Which table is switched on is determined by control bits C12, C13 and C14.

A CCT-IC can contain three sets with 13 language specific characters each: SAA4250 for Englisch, German and Swedish and SAA4250B for Italian, German and French.
The logic levels for the language selection bits C12, C13 and C14 are listed in Table 4.27. If an undefined code is presented, the English set is automatically selected (for SAA4250B German is selected).
For the status of these bits the value that is stored with the page in the memory is used, so that the language changes automatically when another page from the memory is displayed.

The advantage of this method is that more languages can automatically be displayed without intervention by the control microcomputer. Disadvantages, however, are that it is not possible to display several languages on óne page and that locally generated status information is displayed with the character set selected by the broadcasting. These disadvantages can be solved by adding the second addressing method.

The second method is selected/switched on when bit 8 of a data word contains a one. With this method, the total character set is changed. The 128 characters that are addressed by the seven least significant bits of the data word now consist exclusively of display characters and not of display and control characters, as was the case with method 1. The 128 characters that are now available consist of the 96 characters of method 1, in which the German language specific characters are filled in, whereas the remaining 32 characters contain the English and Swedish characters and a number of special status symbols. (With CCT-IC version B, the Italian table is filled in and the French and German characters are available).



* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

38 713 B12

Fig. 4.26

	English	German	Swedish	Italian	Frenc
C12	0	0	0	0	
C13	0	0	1	1	
C14	0	1	0	1	0

Table 4.27

The second method does not use language selection bits C12, C13 and C14. All 128 available characters from the ROM can now be addressed directly.

Both methods can be used in combination to display several languages on one page. If bit 8 is "0", the language selection bits will be followed and if bit 8 is "1", the fixed character set will be used. The information received is written into memory with bit 8 = "0", whereas status information is stored with bit 8 = "1".
Using the additional information that can be transmitted in ghost row 26, the microcomputer can change the stored characters by overwriting them according to the second method. The CCT-IC is capable of receiving the ghost row information, but the set of 128 characters in the CCT-IC does not allow all defined ghost row codes to be executed. The complete character set of the CCT-IC version A is shown in Fig. 4.25, and the set of version B in Fig. 4.26.

4.6.6 Page attributes

The page attributes contain the control bits from the page header of the page. In Table 4.28 a survey is given of all control bits that are indicated with C4 to C14.
In the character generator, use is made of control bits C5, C6, C7, C10, C12, C13 and C14. The page attributes control the character address decoder with respect to the other functions.
With control bits C5 and C6 (news-flash and subtitles), the display characteristics of text and picture are changed over from that from register R5 (normal teletext picture) to that from register R6 (newsflash and subtitling).
With bit C7 the display of row 0 (the page header) can be prevented if it is desirable that the page be displayed without head. The page header does remain stored in the page memory.
With bit C10, the display of rows 0 to 23 can be blanked. Row 24, the status row, is always displayed, regardless of the contents of these control bits.
The language selection bits C12, C13 and C14 switch the adressing of the character address decoder such that the specific characters for the desired language can be selected (see section 4.6.5.).

4.6.7 Addressing the ROM

The line counter circuit supplies addresses to the ROM circuit for the generation of alphanumeric characters.
The counter is clocked with a signal having a repetition frequency of 64 µs (line frequency). The counter normally counts to 10 and its output is used to select a given matrix line of 12 dots in the ROM. When double-height characters are present, the addressing of the ROM is changed such that every line with dots is displayed twice. In this case, the counter counts to 20.
The line counter circuit clocks the row counter circuit which supplies addresses to the memory interface for the reading of the page memory. The row counter normally counts to 25. The status row (row 24) can be displayed above or below the received text by changing the counting **sequence**.
By changing the counting **range**, the upper or lower half of the page (top/bottom) can be displayed double-height (row 0 to 11 or row 12 to 23). If the top or bottom of the page has to be displayed magnified, and the broadcasting also contains control characters for double height, the characters will be displayed quadruple-height. The status row is always displayed in normal (single) height.

4.6.8 Output logic

The output logic circuit (Fig. 4.20) receives serial dot information from the parallel to serial converter and control information from the display control circuit. The features determined with the control information include: foreground and background colour, flashing of characters and blanking.
With the cursor enable signal from the memory interface a cursor can be displayed on the screen for certain applications.
At the position of the cursor, the foreground and background colours are inverted: a red character on a black background is changed into a black character in a red character matrix.

The signals provided by output logic are:
- RGB signals
  These signals contain the red, green and blue components for text display.
- BLAN signal
  This signal blanks the entire TV picture in teletext mode, the character background in mixed mode and the text box.
- Y-signal
  This is a text signal without colour and background information and without flashing function. The signal can be used to control a teletext printer.

The signals are available via buffers with open-drain outputs.

C4: **ERASE PAGE.** This control bit is set to 1 when the information on that page is significantly different from that in the previous transmission of the page.
C5: **NEWSFLASH INDICATOR.** This control bit is set to 1 on a page designated as a news flash page. All information intended for display on such a page will be boxed.
C6: **SUBTITLE INDICATOR.** This bit is set to 1 on a page designated as a subtitle page.
C7: **SUPPRESS HEADER.** The control bit is set to 1 when the page is better displayed without the characters of the page header, row 0.
C8: **UPDATE INDICATOR.** This control bit may be set to 1 when a page contains later information than a previous transmitted page bearing the same page number.
C9: **INTERRUPTED SEQUENCE.** This control is set to 1 when a page is being transmitted out of strict numerical sequence in order to give it priority (such as a subtitle or index page). It allows the page header to be suppressed when rolling headers are displayed to avoid discontinuities in the displayed page numbers.
C10: **INHIBIT DISPLAY.** This control is set to 1 to inhibit the display of meaningless pages.
C11: **MAGAZINE SERIAL.** This bit is set to 1 to display all page headers as rolling headers.
C12, C13, C14: **LANGUAGE SECTION.** These bits are used to display a page using the characters that are specific to a given language area. See table 4.27.

Table 4.28

4.6.9 *Text format and Timing*

A transmitted teletext page consists of 24 rows of 40 characters each. The CCT-IC generates an additional row with status information, extending the display format of the CCT decoder to 25 rows of 40 characters each. To keep the quality of the text as high as possible, the edges of the screen are not used for character display. Consequently only 40 µs of the available active line time of 51,7 µs is used in horizontal direction and 250 of the 287 active lines are used in vertical direction. See Fig. 4.29.

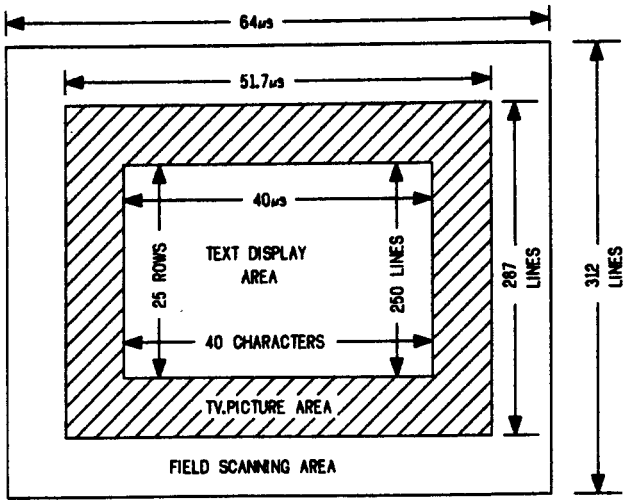


Fig. 4.29

During 40 µs of the line time 40 characters are displayed and during 250 lines 25 rows are displayed. So a character matrix covers 1 µs horizontally and 10 TV lines vertically. The character matrix is filled in according to a 12x10 dot matrix. In general the characters are built up such that at least two dots are always filled in in horizontal direction. Thus the width of the output pulses is at least 1/6 µs, so that the video bandwidth is the same as that of the first-generation decoders.
The double horizontal resolution of this matrix relative to that of the first-generation decoders (6x10 matrix), results in a better shape and better legibility of the characters.

The character information is clocked out of the ROM by means of the 6 MHz F6 clock signal from the Video Input Processor (VIP). Both the leading and the trailing edges of this signal are used for the output frequency of 12 dots per microsecond (12 Mbit/s). The ROM is addressed once per microsecond.

4.6.10 *Display Control*

The display control circuit receives information from the display control and mode registers, page attribute latches, control character decoder and row counter. The information is used to control the text display after the output logic circuit.

Four functions can be controlled: TV picture, text display, text background and contrast reduction. Each of these functions can be switched on or off under software (programme) control. The functions can be stated separately for both inside and outside a box. See appendix B, register information. The control information is stored in register R5 for normal text display and in register R6 for newsflash and subtitles. The use of two registers enables the display parameters that are generally different for both page types to be fixed in advance, so that the control need not intervene at the moment that the page type changes. Boxing by means of "start box" and "end box" characters can be permitted or prevented for certain parts of the screen (R0, R1 to R23 and R24) by means of register R7.
Display Control feeds the contrast reduction signal $\overline{\text{COR}}$ outside. This is a static or character-frequent signal without dot frequency information that can be used to switch a contrast reduction circuit in the TV receiver on and off. For example to display subtitles inside a box with reduced contrast. The signal can also be used as a static signal to switch on mixed-mode, just as the superimpose output of the first-generation decoders.
The $\overline{\text{COR}}$ signal is switched on and switched off, inside and outside the box respectively, with the bits COR IN and COR OUT of registers R5 and R6 (see appendix B).

4.7 Memory Interface Function

4.7.1 Block diagram

The Memory Interface arranges the communication between the CCT-IC and the external page memory. The circuit provides data, address and control signals to write received teletext information in the memory, to read this information back for display on the screen and to write information into, or read information from the memory via the IIC bus. A maximum of 8K x 8 bits of static or pseudostatic RAM can be connected in multiples of 1K x 8 bits.
In Fig. 4.30 the block diagram of the Memory Interface is shown. The data that must be written into the memory is provided by the Acquisition function (received teletext data) and by the IIC Bus interface (status information of the microcomputer). The multiplexer (MUX) can transmit one of both data sources to the eight data lines D0 to D7 via the 3-state output buffers. These eight data lines are used bidirectionally, that is, both for writing and reading information. During reading, the information on the lines is passed on, via the input buffers, to the character generator and the IIC bus interface. The 3-state output buffers are then in the high-impedance position.

The memory is addressed via the 13 address lines A0 to A12. These lines are buffered by buffers with push-pull outputs. Ten of these address lines (A0 to A9) are used to address the 1024 locations in a memory page (chapter). In the maximum configuration, eight of these memory pages are available, divided among two banks of four pages each. Address line A12 is used to select the bank and address lines A10 and A11 to select one of the four pages inside the bank. Address lines A0 to A9 are generated by the address mapping circuit on the basis of column and row information from the acquisition circuit, the IIC interface, the Timing Chain and the character generator in the CCT-IC.

The control signal $\overline{OE}$ (Output Enable) is rendered active low when data must be read from the memory. The signal is passed on to the corresponding pin of the memory IC to activate the 3-state output buffers of this IC. When $\overline{OE}$ is active, the output buffers of the Memory Interface remain switched off to prevent bus conflicts on the data lines.

The $\overline{WE}$ (Write Enable) signal is used to write data in the memory. The signal is active "low" and is generated by the write control circuit with the aid of timing signals from the Memory Timing Generator and write signals from acquisition circuit and IIC interface. The Memory Timing Generator allots times for the execution of the various functions and controls the various multiplexes (MUX) with which address and data sources are selected.

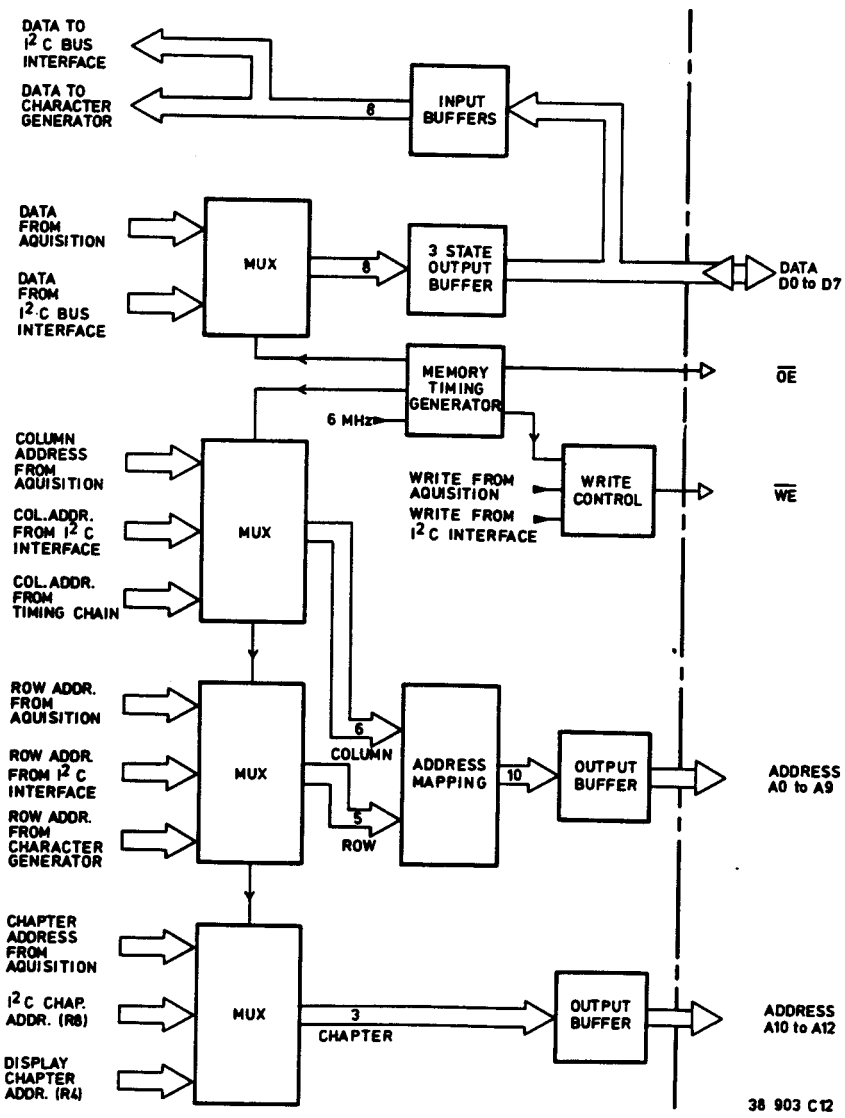


Fig. 4.30

The Memory Interface has been designed such that teletext data can be read and written simultaneously during the same line period. This is necessary for non-interlaced display and in so-called Full Channel mode when teletext information is transmitted on every line in the field.
The line period of 64 µs is therefore divided into 128 periods of 500 ns. These periods are alternately used for a write and a read cycle. The write cycles always start a whole number of microseconds after the line synchronization, whereas the read cycles always start at multiples of half microseconds. See Fig. 4.31.

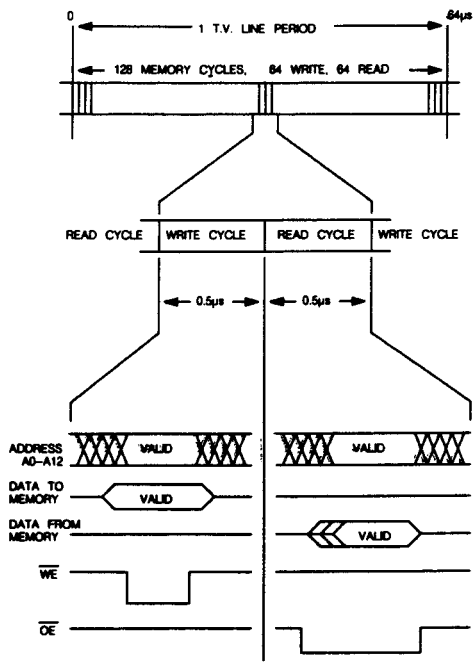


Fig. 4.31 PRS.00767

4.7.2 *Memory Configuration*

In principle, the external memory can be connected directly to the interface pins of the CCT-IC, that is, without extra components. If, however, the memory is made up of several memory ICs, address lines A10, A11 and A12 will have to be converted, in an external selection circuit, into chip select signals for the various memory ICs. If not the maximum memory is connected, address lines A10, A11 or A12 can be left unused (open). Address line A12 is always connected in a decoder which can also receive ghost rows, because, in that case, A12 changes between normal and ghost row data. In a ghost row decoder in minimum configuration (2K x8 bits memory), A12 is connected with address line A10 of the memory IC.
In a normal decoder, without ghost row reception, address line A12 is controlled by the bank select bit from the acquisition circuit. For the addressing of the memory, the address lines in a normal decoder are used consecutively.

5. PAGE MEMORY

5.1 Circuit diagram

IC 7102 (MSM2128-20) is a so-called static Random Access Memory (RAM) which is used by the CCT-IC for the storage of page information. The IC has a memory capacity of 2048 8-bit words (2K bytes) and is fully controlled by the memory interface function of the CCT-IC.
The 2048 memory words are addressed by means of the 11 address lines A0 to A10. Data is transported bidirectionally via the 8 data lines D0 to D7, whereas the direction of the data (reading or writing) is determined by the control lines $\overline{OE}$ and $\overline{WE}$.
The IC operates from a 5 V power supply.

5.2 Control

Table 5.1 presents the function truth table of the control signals. The chip select input (pin 18) is connected to earth and hence is always active.

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	mode	output	
H	X	X	not selected	high Z	stand by
L	L	X	write	high Z	active
L	H	L	read	data out	active
L	H	H	not selected	high Z	active

H = high level
L = low level
X = don't care
Z = impedance

Table 5.1

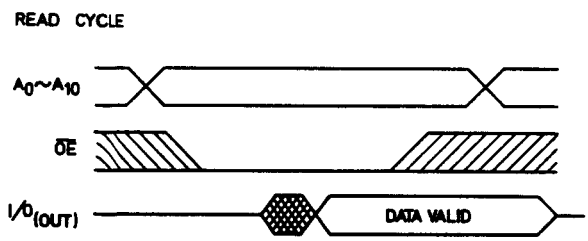


Fig.5.2

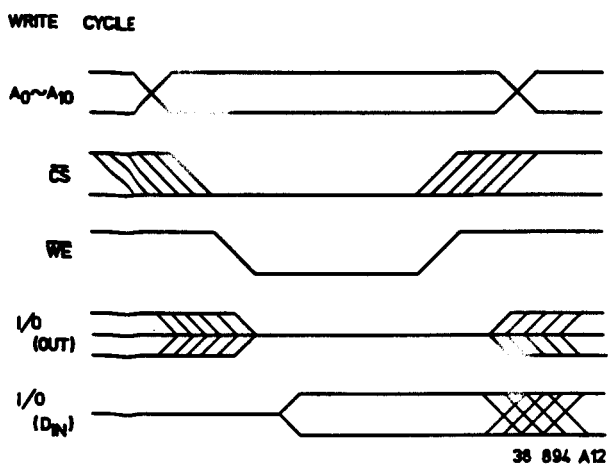


Fig. 5.3

5.3 Reading data

The timing is given in Fig. 5.2.
The address of the memory location to be read is applied to address inputs A0 to A10 of the memory IC. The contents of the addressed memory location are put on data lines D0 to D7 by rendering control output $\overline{OE}$ (Output Enable) low. The Write Enable ($\overline{WE}$) input is high during reading. The read action is ended by rendering $\overline{OE}$ high again.

5.4 Writing data

The timing is given in Fig. 5.3.
Data can be written into memory by addressing a memory location with address lines A0 to A10 and by rendering the $\overline{WE}$ (Write Enable) line low. The data applied on data lines D0 to D7 is written in the addressed memory location.
The logic level of the $\overline{OE}$ line is not important during writing. This is realized by the input circuit for the control signals. See figure 5.4 and table 5.5.

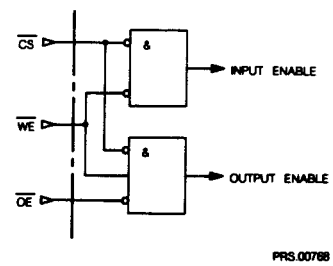


Fig. 5.4

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	input	output
H	X	X	L	L
L	H	H	L	L
L	L	X	H	L
L	H	L	L	H

X = don't care
H = high level
L = low level

Table 5.5

6. INPUT AND OUTPUT CIRCUITS

6.1 MIBUS circuit

MIBUS stands for Mullard Instruction Bus and consists of two lines: DATA and DLIM. This bus is used to apply the user-stated control information from the TRD4 control circuit of the television to the teletext decoder. The DATA signal contains the actual information; the DLIM signal is the clock (Fig. 6.1).
DLIM is fed to B-TS7109 via plug 4V4 and R3109. If DLIM is low, the transistor will cut off. In that case, C-TS7109 and pin 12-IC7105 will be high (+5 Volts) via R3111. If DLIM is high, the transistor will be driven into saturation. C-TS7109 and pin 12-IC7105 then are low. The transistor inverts the DLIM signal.

DATA is applied via plug 3V4 and R3112. Diodes D6103 and D6104 limit possible peaks in the signal amplitude between about 5,7 and -0,7 volts. If the signal amplitude exceeds +5 V, D6103 will start to conduct. This causes the amplitude on pin 25-IC7105 to be clipped at about +5,7 V. If the signal amplitude drops below 0 Volts (ground level), D6104 will start to conduct. This causes the amplitude on pin 25-IC7105 to be clipped at about −0,7 V.

6.2 R,G,B circuit

The output buffers for R, G and B signals (see Fig. 6.2) fulfil an interface function between the outputs of the CCT-IC and the Teletext interface of the TV receiver.
The output buffers are formed by emitter followers TS7118, TS7119 and TS7121, which are controlled by the open-collectors outputs of the CCT-IC. The pull-up voltage at the output collectors is determined by the circuit with TS7115. This voltage, which is adjustable with potentiometer 3146, determines the brightness of the text on the screen. The voltage on the wiper of potentiometer 3146 is adjustable between 4,7 V and 2,6 V.
The voltage at the emitter of TS7115 is about 0,6 V higher and lies between 5,3 V and 3,2 V. Zener diode D6105 stabilizes the voltage across potentiometer R3146 at about 4,7 V, to avoid that variations in the +13C supply voltage appear on the screen as variations in the brightness of teletext. When the pull-up voltage is changed, the RGB signals are affected in the same degree, causing the white-level (brightness) of the text to change.

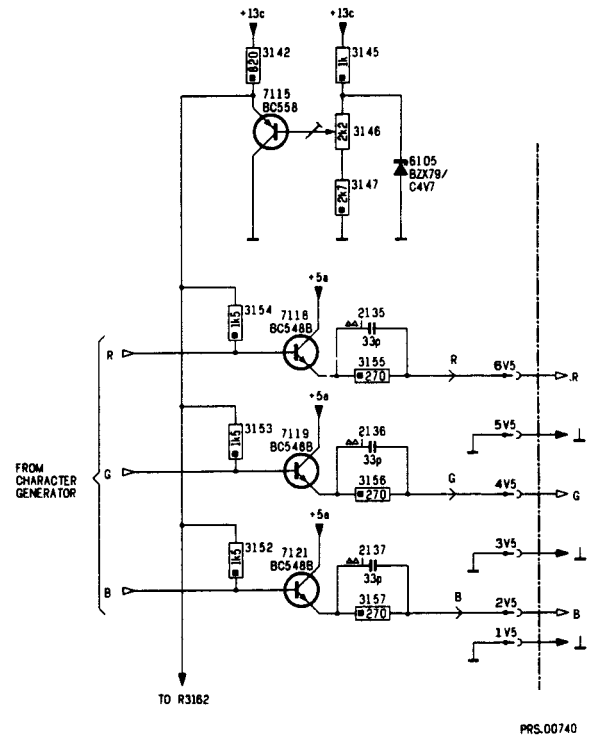


Fig.6.2

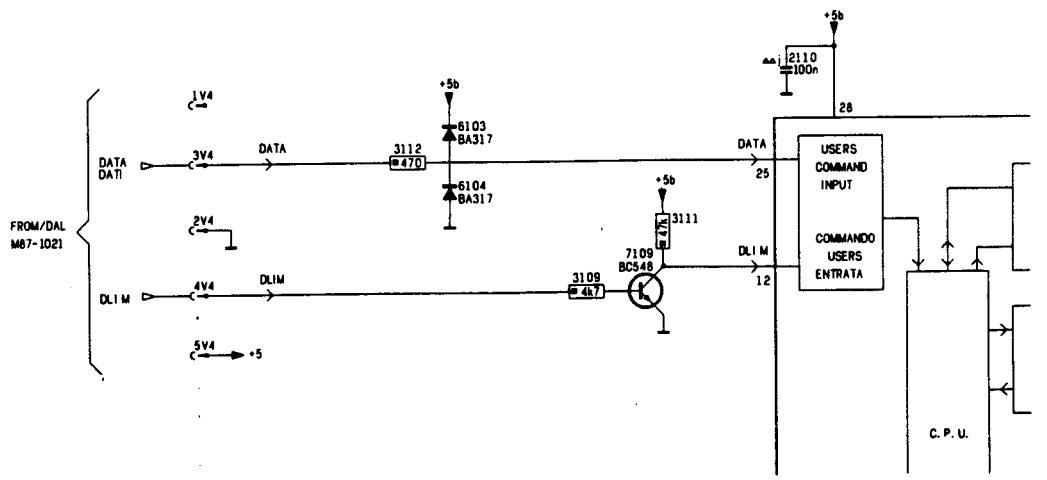


Fig. 6.1

6.3 Auto Interlace Circuit

The circuit surrounding TS7122 and TS7123 (Fig. 6.3) is controlled by the PO (Picture On) and the $\overline{O}$/E signal (Odd/even) from the CCT-IC. PO is high when the TV picture is being displayed, with or without teletext (subtitles, newsflash, etc.). PO is low in TXT mode. $\overline{O}$/E is low when the odd field is displayed and high when the even field is displayed.
When PO is low (in TXT mode), the $\overline{O}$/E signal will switch transistor TS7122 on at even fields and off at odd fields.
If TV picture is being displayed, TS7122 will be conducting. If TS7122 conducts, TS7123 will cut off and vice versa. If TS7123 conducts a small DC current will flow through the vertical deflection coil, causing the off field to shift one line up. Consequently, the even and the odd field overlap, causing the annoying jumping of the text as a result of interlacing to disappear in teletext mode.
In MIX mode, when TV picture and text are simultaneously displayed, the jumping of the text is not annoying. Consequently, the interfacing will not be switched off in this mode.

6.4 Blanking circuit

The blanking signal (Fig. 6.4) is transmitted to the teletext interface of the TV receiver for blanking of the TV picture, by transistor TS7116 which is switched as emitter follower. R3149 is a pull-up resistor for the open-collector output of the BLAN signal. The CCT-output circuit of the blanking signal contains a short-circuit protection that becomes operative when the open-collector output of the BLAN signal is shorted to ground. This may occur at flash-overs in the picture tube. When the short-circuit protection circuit is switched on, the blanking output will adopt a logic high level (blanking), causing the picture display to be blanked. To switch the short-circuit protection circuit off again, the blanking output should be provided with a logic low level. This low level is obtained by driving TS7124 into conduction. Every two fields, TS7124 is switched on for a short moment by the positive flanks in the $\overline{O}$/E signal.

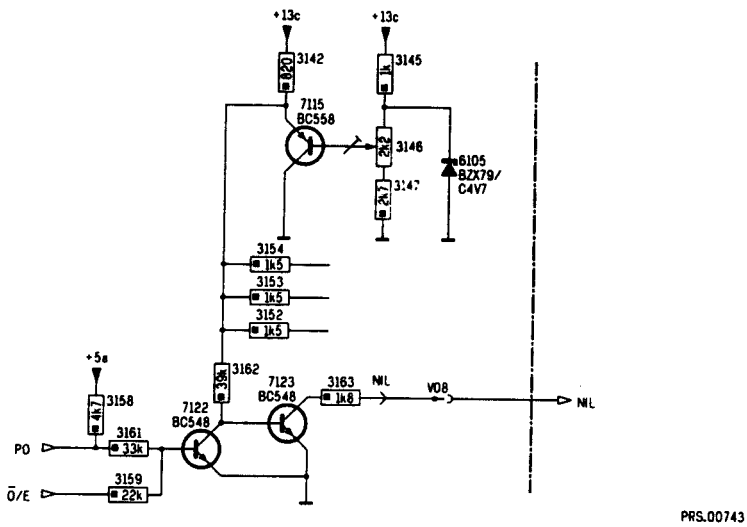


Fig. 6.3

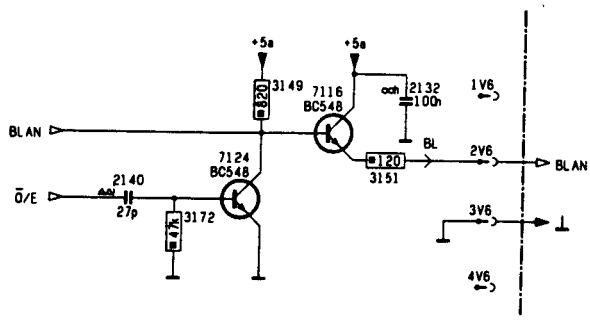


Fig. 6.4

APPENDIX

A IIC Bus

Introduction

IIC or I²C stands for Inter IC Bus. This is a standard bus for data transmission between two or more ICs. The bus consists of a data and a clock line, designated by SDA (serial data) and SCL (serial clock) resp.; see Fig. 1.

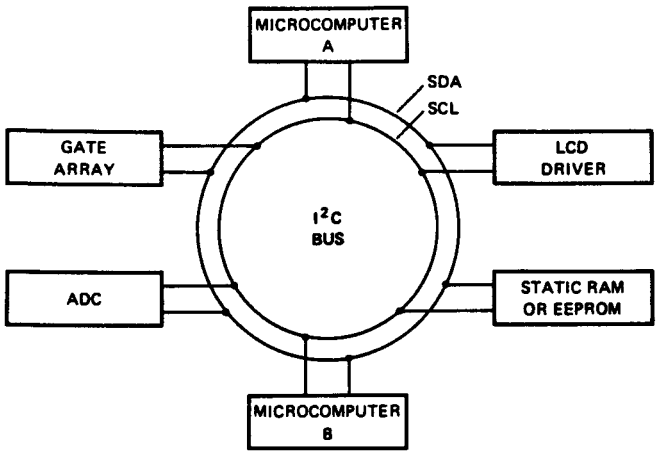


Fig. 1

Dependent on its function an IC may act as transmitter and/or as receiver. A display may for instance act exclusively as receiver; a memory, however, may be both transmittter and receiver.

Apart from as "transmitter" and "receiver" ICs may also act as "master" or "slave". The master starts the data transmission on the bus and generates the clock signals for transmission. The IC that is addressed will always be the slave. All ICs that communicate with each other via the bus possess a unique address.
Because it is possible that several ICs simultaneously want to use the bus, an arbitration procedure has been built in. This procedure is based on the wired-AND connection of all ICs to the IIC bus. Arbitration takes place on the SDA line. When two or more masters simultaneously deliver data to the bus, the arbitration will be lost by the master that puts a high level (one) on the bus while the other delivers a low level (zero). Namely, its transmitted level does not correspond with the level on the bus then.

IIC terminology

Master	The IC that starts data transmission, produces the required clock and ends the transmission. The master may transmit or receive data.
Slave	The IC that is addressed by the master. The slave may transmit or receive data.
Transmitter	The IC that transmits data via the bus.
Receiver	The IC that receivers data via the bus.
Multi-master	Several masters may activate the bus.
Arbitration	Procedure to ensure that when several masters simultaneously start to use the bus, only one gets to use the bus without data distortion.
Synchronization	Procedure to synchronize the clock signals of two or more ICs.
Acknowledge	Confirmation from the receiver to the transmitter that a byte (8 bits) has been received.

Bus connection

Both SDA and SCL are bidirectional lines that are connected to a positive power supply voltage via a resistor (Fig. 2). When the bus is free, both lines are high. The output stages of the ICs that are connected to the bus possess an open drain or open collector to obtain a wired-and function on the bus.
The number of ICs to be connected to the bus is limited only by the maximum bus capacity of 400 pF. Data on the IIC bus can be transferred at a speed of 100 Kbits/s.

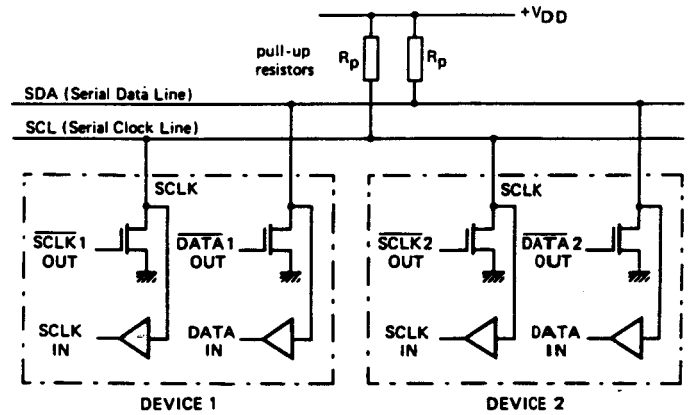


Fig. 2

Data transmission

Data transmissions follow the format as indicated in Fig. 3. After a start condition the slave address is sent. The first seven bits of this address byte give the slave address, the eight bit (L.S.B.) determines the direction of the message. A "0" means that the master wants to write information to the selected slave. A "1" means that the master wants to read information from the slave.

Each byte that is sent via the SDA line of the bus is 8 bits long. The number of bytes to be sent per transmission is unlimited. Each byte should be followed by an acknowledge bit. Data are transmitted with the most significant bit (MSB) first.

A data transmission is terminated by a stop condition, generated by the master. If the master wants to continue communication via the bus, it may generate a new start condition and address another slave without first generating a stop condition (see Fig. 4). In this way various combinations of read/write formats are possible within a transmission.

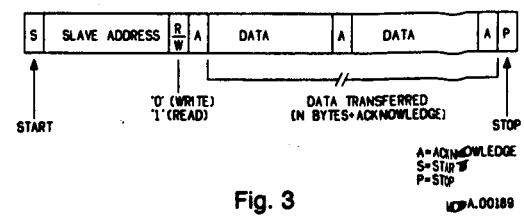


Fig. 3

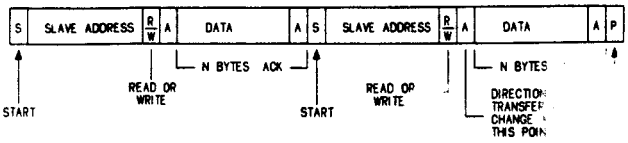


Fig. 4

Timing

A clock pulse is generated with each data bit that is transmitted (see Fig. 5). The data on the SDA line should be stable during the "high" period of the clock. The high or low status of the data line may only be changed when the clock signal of the SCL line is low.

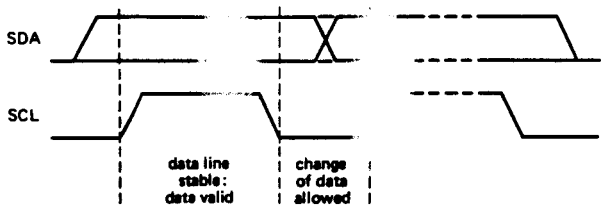


Fig. 5

Start and Stop conditions

Start and Stop conditions are generated by the master at the beginning and at the end of a data transmission resp. (see Fig. 6). The bus is considered busy after a start condition and free after a stop condition. A start condition is a high to low transition of SDA while SCL is high. A stop condition is a low to high transition of SDA while SCL is high.

Acknowledge

With data transmission acknowledge is obligatory. The clock pulse for the acknowledge bit is generated by the master. The transmitter leaves the SDA line free (high) during the acknowledge clock pulse. Next the receiver should render the SDA line low so that the SDA line will be stably low during the high period of this clock pulse. If no acknowledge is given by the receiver (the SDA line is left high), the master may generate a stop condition to reject the transmission.
The total data transmission is given in Fig. 8.

Wait condition

If during data transmission the receiver can temporarily not receive a new data byte, for instance because the previously offered data should first be processed, the receiver can place the transmitter in the wait mode by keeping the SCL line low.

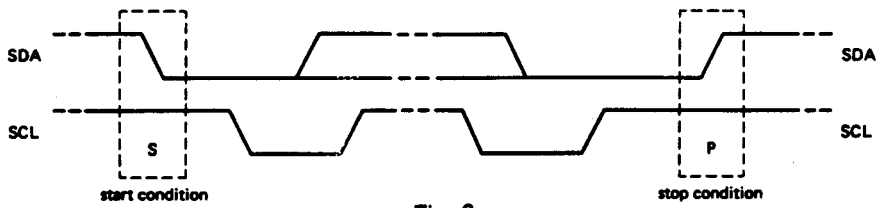


Fig. 6

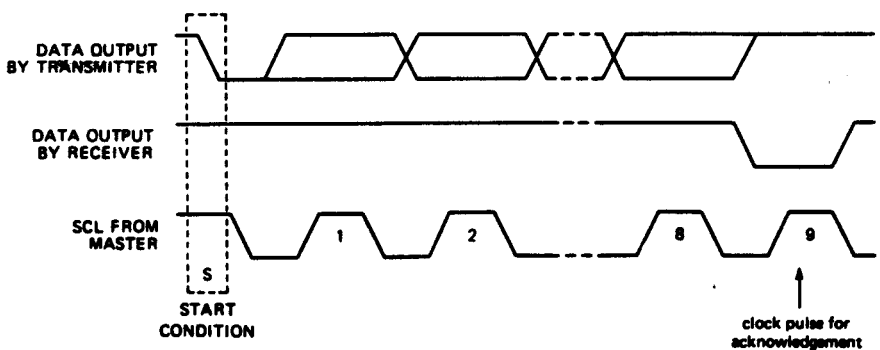


Fig. 7

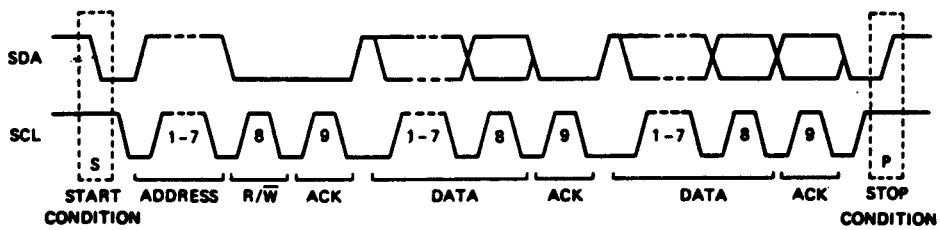


Fig. 8

APPENDIX

B. CCT REGISTER FUNCTIONS

Introduction

The CCT IC contains eleven registers controlling the various functions of the IC. A survey is given in Fig. 1.

R1 mode register

The subaddress of R1 is 0000 0001

D7	D6	D5	D4	D3	D2	D1	D0
TA	$\overline{7+P}$/ 8 bit	acq. $\overline{on}$/off enable	ghost row enable	$\overline{DEW}$/ full field	TCS on	T1	T0

This register determines the way in which acquisition and display of the text are performed. The register is set by the control microcomputer.
The meaning of the bits is as follows:

T1,T0	These bits determine if the TCS signal delivers an interlaced or a non- interlaced composite sync signal.
TCS ON	This bit switches the TCS output buffer on (TCS ON = 1) or off (TCS ON = 0).
$\overline{DEW}$/FULL FIELD	A "0" on this bit switches the decoder in the field flyback mode. Here teletext data is accepted only during the Data Entry Window (DEW) period (lines 6 through 22 of each field). A "1" on this bit selects the FULL FIELD mode in which data is accepted on all TV lines.
GHOST ROW ENABLE	Choice between normal and ghost row mode. In the ghost row mode, apart from the normal teletext rows, ghost rows are acquired too. In the ghost row mode 2 memory pages (chapters) (2K x 8 bits) are used per teletext page.
ACQ $\overline{ON}$/OFF	Switching on and off of the acquisition function. The acquisition function is switched on for the acquisition of teletext. The function is switched off for display of e.g. viewdata or telesoftware information.
$\overline{7+P}$/8 BIT	Switching on and off the parity check on the received teletext data. In $\overline{7+P}$ mode the teletext data bytes should consist of 7 data bits and 1 parity bit. After parity checking the 7 data bits are written in the memory. In the 8-bit mode all 8 bits of the data bytes are without parity checking written in the memory.
TA	Text bit which should be "0" for normal operation of the CCT-IC.

After the bits of R1 have been set, R2 is addressed automatically.

R2 Address register for page request

The subaddress for R2 is 0000 0010

D7	D6	D5	D4	D3	D2	D1	D0
-	bank select A2	ACQ CCT A1	ACQ CCT A0	TB	start column SC2	start column SC1	start column SC0

All bits in this register are "0" after the power supply has been switched on.

This register contains addressing information with respect to page request. The register is set by the control processor to request a new page.
The meaning of the bits is as follows:

START COLUMN SC0, SC1, SC2	These three bits indicate which subregister of Register R3 is addressed first in case of a later to be given writing action to Register R3.
TB	Mode bit for testing purposes which should be "0" for normal operation of the CCT-IC.
ACQ.CCT A1,A0	These two bits determine which of the four acquisition circuits is selected for the search of a requested page. The bits control address lines A11 and A10 upon reception of the requested page.
BANK SELECT A2	In normal mode (no ghost row mode) this bit determines which bank of 4 memory chapters is addressed. The bit controls address line A12 upon reception of the requested page.

After the bits of R2 have been set, Register R3 is addressed automatically.

R3 Data Register for page request

This register has subaddress 0000 0011

	D7	D6	D5	D4	D3	D2	D1	D0
C0	-	-	-	do care magazine	$\overline{HOLD}$	MAG2	MAG1	MAG0
C1	-	-	-	do care page tens	PT3	PT2	PT1	PT0
C2	-	-	-	do care page units	PU3	PU2	PU1	PU0
C3	-	-	-	do care hours tens	-	-	HT1	HT0
C4	-	-	-	do care hours units	HU3	HU2	HU1	HU0
C5	-	-	-	do care minutes tens	-	MT2	MT1	MT0
C6	-	-	-	do care minutes units	MU3	MU2	MU1	MU0

All bits in this register are "0" after switching on of the power supply.

Register 3 consists of the 7 subregisters C0 through C6. These subregisters contain the data for page request. The registers are set successively by the controlling microcomputer beginning with the subregister indicated by the START COLUMN bits from register R2.

SUBREGISTER NO / REGISTER NO		D7	D6	D5	D4	D3	D2	D1	D0	REGISTER FUNCTIONS
R1		TA	$\overline{7+P/8\ BIT}$	ACQ $\overline{ON/OFF}$	GHOST ROW ENABLE	$\overline{DEW}$/ FULL CHANNEL	TCS ON	T1	T0	MODE CONTROL
R2		—	BANK SELECT A2	ACQ. CCT A1	ACQ CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	PAGE REQUEST ADDRESS
R3	C0	—	—	—	DO CARE	$\overline{HOLD}$	MAG2	MAG1	MAG0	PAGE REQUEST DATA (MAGAZINE)
R3	C1	—	—	—	DO CARE	PT3	PT2	PT1	PT0	PAGE REQUEST DATA (PAGE TENS)
R3		—	—	—	DO CARE	PU3	PU2	PU1	PU0	PAGE REQUEST DATA (PAGE UNITS)
R3	C3	—	—	—	DO CARE			HT1	HT0	PAGE REQUEST DATA (HOURS TENS)
R3	C4	—	—	—	DO CARE	HU3	HU2	HU1	HU0	PAGE REQUEST DATA (HOURS UNITS)
R3	C5	—	—	—	DO CARE		MT2	MT1	MT0	PAGE REQUEST DATA (MINUTES TENS)
R3	C6	—	—	—	DO CARE	MU3	MU2	MU1	MU0	PAGE REQUEST DATA (MINUTES UNITS)
R4		—	—	—	—	—	A2	A1	A0	DISPLAY CHAPTER
R5		BK GND OUT	BK GND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	DISPLAY CONTROL NORMAL
R6		BK GND OUT	BK GND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	DISPLAY CONTROL NEWSFLASH /SUBTITLE
R7		STATUS ROW $\overline{BTM/TOP}$	CURSOR ON	$\overline{CONCEAL/REVEAL}$	$\overline{TOP/BOTTOM}$	$\overline{SINGLE/DOUBLE\ HEIGHT}$	BOX ON 24	BOX ON 1–23	BOX ON 0	DISPLAY MODE
R8		—	—	—	—	CLEAR MEMORY	A2	A1	A0	ACTIVE CHAPTER
R9		—	—	—	R4	R3	R2	R1	R0	ACTIVE ROW
R10		—	—	C5	C4	C3	C2	C1	C0	ACTIVE COL
R11		D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	ACTIVE DATA

— Bit does not exist

Auto increment

Fig. 1

PRS.00761

The meaning of the bits is as follows:

MAG0,1,2	Magazine number (a hundred) of the page to be requested.
$\overline{\text{HOLD}}$	Stop acquisition bit.
DO CARE	Bit indicating if the contents of this subregister should be involved in the acquisition.
PT0,1,2,3	Tens of the page number.
PU0,1,2,3	Units of the page number.
HT0,1	Thousands of the subcode.
HU0,1,2,3	Hundreds of the subcode.
MT0,1,2	Tens of the subcode.
MU0,1,2,3	Units of the subcode.

When the power supply is switched on, all bits from this register are set to zero. The consequence is that the acquisition circuits are, as a result of the $\overline{\text{HOLD}}$ bit, at "stop". ALL DO CARE bits also are zero, so that in case of request of normal pages the subcode digits need not be addressed.

After register R3 has been set the next register is not addressed automatically.

R4 Selection register for memory pages

This register has subaddress 0000 0100

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	A2	A1	A0

All bits in this register become "0" upon switching on of the power supply. This register is set by the control processor in a multipage decoder as a result of control commands by the user.

The meaning of the bits are as follows:

A0,A1,A2	These three bits are used to indicate which of the eight memory pages (chapters) should be displayed on the screen. During memory read cycles these bits correspond with the logical levels at address lines A10, A11 and A12 resp.

After the bits in register R4 have been set Register R5 is addressed automaticallly.

R5 Control register for text display (normal)

This register has subaddress 0000 0101

D7	D6	D5	D4	D3	D2	D1	D0
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN

Upon switching on of the power supply bits PON OUT and PON IN are set to "1", while the other bits are rendered "0".

The functions that are controlled by this register can be divided in two groups: functions applying within (IN) a box and functions applying outside a box (OUT). The register controls the text display on the screen only if the page to be displayed is no newsflash or subtitle page.

The meaning of the bits is as follows:

PON IN, PON OUT	These bits determine if the TV picture is displayed inside and outside the box respectively. The function controls the BLAN pin (high to blank the TV picture). A "1" in the register means that the TV picture is displayed, a "0" means that the TV picture is blanked. The function BKGND (background) in bits D6 and D7 has priority over this function.
TEXT IN, TEXT OUT	These bits determine if text is displayed inside and outside the box respectively. A "1" means "display text", a "0" means "do not display text".
COR IN, COR OUT	These bits determine if the picture contrast inside and outside the box respectively is reduced (COR = Contrast Reduction). A "1" means reduced contrast, a "0" means normal contrast. This function controls the COR pin.
BKGND IN, BKGND OUT	These bits determine if background colours of the text are displayed inside and outside the box respectively. A "1" means: both background and foreground display. A "0" means: only foreground (text) display. This function has priority over the PON function (bits 0 and 1).

Examples of the use of these functions are given with the description of register R6.

After the bits of register R5 have been set register R6 is addressed automatically.

R6 Control register for text display (newsflash and subtitle)

This register has subaddress 0000 0110

D7	D6	D5	D4	D3	D2	D1	D0
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN

Upon switching on of the power supply bits PON OUT and PON IN are set to "1" while the other bits are rendered "0".

In structure and function this register is identical with register R5. The register controls the text display on the screen if the page to be displayed is a newsflash or subtitle page (control bit C5 or C6 from the page header is "1").

The use of two separate control registers for text display (R5 and R6) makes it possible to preset the display characteristics of both types of pages. If the type of page changes, intervention of the microcomputer will not be required.

After the bits of register R6 have been set register R7 is addressed automatically.

Examples of the use of the functions of R5 and R6.

	BKGND		COR		TEXT		PON	
	OUT	IN	OUT	IN	OUT	IN	OUT	IN
a)	0	0	0	0	0	0	1	1

This setting gives TV picture without teletext display.

	BKGND		COR		TEXT		PON	
	OUT	IN	OUT	IN	OUT	IN	OUT	IN
b)	1	1	0	0	1	1	0	0

This setting gives only teletext display.

	BKGND		COR		TEXT		PON	
	OUT	IN	OUT	IN	OUT	IN	OUT	IN
c)	0	0	1	1	1	1	1	1

This setting gives teletext display combined (MIXED) with a TV picture reduced in contrast. Boxing is not done.

	BKGND		COR		TEXT		PON	
	OUT	IN	OUT	IN	OUT	IN	OUT	IN
d)	0	0	0	1	0	1	1	1

This setting gives display of TV picture combined with display of boxed teletext. Inside the box the TV picture is displayed with reduced contrast (improved display of subtitle).

R7 Display Mode Register

This register has subaddress 0000 0111

D7	D6	D5	D4	D3	D2	D1	D0
status row $\overline{\text{btm/top}}$	cursor on	$\overline{\text{conceal}}$/ reveal	$\overline{\text{top}}$/ bottom	$\overline{\text{single}}$/ double height	box on 24	box on 1-23	box on 0

All bits in this register are set to "0" upon switching on of the power supply.

This register is filled in by the microcomputer before text is displayed. The contents can be changed as a result of control commands by the user.

The meaning of the bits is as follows:

BOX ON 0	A "1" in this bit allows boxing in row 0.
BOX ON 1-23	A "1" in this bit allows boxing in rows 1 through 23.
BOX ON 24	A "1" in this bit allows boxing in row 24.

The BOXing function controls are intended to give flexibility in case of status displays on the screen. Their working depends on the presence of the control character BOX ON and BOX OFF and on the status of display control registers R5 and R6.
Example: The status row (row 24) can use boxed text to display the decoder status. To suppress the boxed text from the status row in decoder status. To suppress the boxed text from the status row in case of subtitle display BOX ON 1-23 should be set to "1" and BOX ON 24 to "0". And conversely, status display in the TV picture can be obtained by rendering BOX ON 24 "1". Rendering BOX ON 1-23 "0" prevents newsflash or subtitle pages that have been stored in the memory from becoming visible on the screen.

$\overline{\text{SINGLE}}$/DOUBLE HEIGHT	This bit sees to switch-over between normal (single) and double character height. The characters in row 24 (status row) are always displayed in single height.
$\overline{\text{TOP}}$/BOTTOM	Choice between display in double height of row 0-11 or rows 12-23. The status of this bit is only important if double character height has been selected with the previous bit.
$\overline{\text{CONCEAL}}$/ REVEAL	A "0" on this bit allows control character CONCEALED DATA to be recognized by the decoder. As a result the concealed characters are displayed as spaces. A "1" on this bit prevents recognition of this control character. The concealed characters are displayed normally.
CURSOR ON	If this bit is "1", a cursor is displayed on the screen. The cursor is controlled by the IIC Interface and Control function of the CCT IC.
$\overline{\text{STATUS}}$ ROW BTM/TOP	Row 24, the status row, is displayed below the main text if this bit is "0". If this bit is "1", the status line is displayed above the main text. Text display starts with row 24, followed by rows 0, 1, 2, ... 23.

After register R7 has been set a next register is not addressed automatically.

R8 Active memory page register

This register has subaddress 0000 1000

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	clear memory	A2	A1	A0

Upon switching on of the power supply A0, A1 and A2 are rendered "0".

In combination with R9 and R10 this register is used by the control microcomputer to write data to or to read data from the page memory.
The meaning of this bits is as follows:

A2,A1,A0	These three bits select the memory page (chapter) that will be used for data transfer via the IIC bus. The three bits control address pins A12, A11 and A10 respectively during the reading or writing action via the IIC bus. This chapter address is completely independent of the chapter that has been selected for display (in R4) and for acquisition (in R2).
CLEAR MEMORY	This bit is not kept stored in the register. If a "1" is written to this bit, the memory chapter that has been addressed in this register is erased. All memory locations from row 0, character 0, to row 25, character 23 (Fig. 4.15) are filled with spaces (character code 0010 0000). Execution of this function may take 22 ms.

After writing to register R8 register R9 is addressed automatically.

R9 Active text row register

This register has subaddress 0000 1001

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	R4	R3	R2	R1	R0

Upon switching on of the power supply all bits in this register are rendered "0".

In combination with R8 and R10 this register is used by the controlling microcomputer to write data to or to read data from the page memory. The meaning of the bits is as follows:

R4, R3, R2, R1, R0 — These five bits select the memory row that will be used for data transfer via the IIC bus. Only row numbers 0 through 25 are valid.

The contents of register R9 is automatically incremented by 1 when the contents of register R10 changes from 39 to 0. After row 23 row 0 is addressed. Rows 24 and 25 can only be addressed by writing the row number directly in register R9.
After R9 has been set register R10 is addressed automatically.

R10 Active column register

This register has subaddress 0000 1010

D7	D6	D5	D4	D3	D2	D1	D0
-	-	C5	C4	C3	C2	C1	C0

Upon switching on of the power supply all bits are rendered zero.

This register is, in combination with R8 and R9, used by the controlling microcomputer to write data to or to read data from the page memory. The meaning of the bits is as follows:

C5, C4, C3, C2, C1, C0 — These 6 bits contain the column address that will be used for data transfer via the IIC bus. Only column numbers 0 through 39 are valid. The column number will increment automatically be incremented after each reading or writing action to active data register R11. Column number 39 increments to column number 0.

After register R10 has been set register R11 is addressed automatically.

R11 Active data register

This register has subaddress 0000 1011

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

In combination with registers R8, R9 and R10 this register is used by the microcomputer to write data to or read data from the page memory. The meaning of the bits is as follows:

D7...D0 — These eight bits represent the data contents of the memory location that has been selected by registers R8, R9 and R10. R8 selects the memory chapter, R9 selects the row within the memory chapter and R10 determines the column (the character) within the selected row.
Bits D7 through D0 are read/write bits. As a result data already present in the memory can be read with a read command via the IIC bus. It is also possible to write new data with a write command via the IIC bus in the selected memory location.

After writing of a data byte to, or reading of a data byte from register R11, the contents of register R10 (and if necessary R9 and R8) increments automatically. Addressing of a new register does not take place automatically.

APPENDIX

D List of terms and abbreviations

This list gives a survey of the most important terms and abbreviations from this circuit description, together with a brief elucidation. The elucidations do not contain general definitions but give only the meaning of the terms and abbreviations within the scope of this circuit description.

A	Acknowledge; confirmation of reception of a data byte in case of IIC-bus transfers.
Acquisition	Acquisition of teletext data from the TV signal.
BLAN	Blanking; picture suppression signal delivered by the CCT-IC.
Blanking	Suppression of the TV picture on the screen.
CBB	Colour Burst Blanking; part of the SAND-signal for suppression of the colour synchronisation signal (colour burst) at the beginning of the TV line.
CCT	Computer Controlled Teletext; reception of Teletext under control of a microcomputer.
CCT-IC	Integrated circuit type SAA 5241A or SAA 5241B. Sees to all digital functions with respect to the processing of the teletext signal.
CCT-decoder	Teletext decoder based on the CCT IC.
COR	Contrast Reduction; control signal from the CCT IC. Among other things, this signal can be used to switch on/off a circuit which reduces the picture contrast. In this way improved legibility of the text in MIX mode is obtained. In the system-4 decoder the signal is used to switch on/off the interlacing.
CPU	Central Processor Unit; central data processing part of a microcomputer.
CVBS	Composite Video Blanking Sync; signal containing the non-modulated Video Blanking and Synchronization data from the TV signal. The CVBS signal is used as source of information for the teletext decoder.
DATA	Information signal; serial data signal from the Mullard Instruction Bus (MIBUS). Contains teletext control data and is delivered by the control system of the TV.
DATA SLICER	Circuit within the Video Input Processor that retrieves the digital teletext signal from the CVBS signal.
DC	Direct Current.
DLIM	Data Limiter; serial clock signal from the Mullard Instruction Bus (MIBUS). Is delivered by the control system of the TV.
F6	Frequency 6 MHz; clock signal from VIP2 having a frequency of 6 MHz. The F6 clock is synchronized to the TV signal and is used as time base for text display on the screen.
Flash-over	in the picture tube. Results in electromagnetic interference pulses that may cause disturbances in the circuits of the TV.
Ghost Rows	Additionally transmitted teletext rows with extra control data. These rows cannot be received, (are not identified) by first generation teletext decoders, hence the name ghost rows. The CCT decoder is capable of receiving these rows.
Hamming Code	Way of coding of data bytes in which data bits are combined with protection bits. Thus it is possible to identify per byte multiple transmission errors and to identify and correct single transmission errors (1 bit error per byte).
HF	High Frequency;
HOK	Hamming bytes O.K.; output signal from the CCT IC. This signal indicates if the teletext data bytes coded in Hamming that are presented to the CCT IC, contain multiple (i.e. incorrigible) errors.
IC	Integrated Circuit.
IIC-bus	Inter IC bus; serial bus system for data transmissions between ICs and circuits within a set. The IIC bus makes use of a data line (SDA) and a clock line (SCL). Transmissions take place according to fixed procedures.
Interface	Circuit to interconnect the input and output of two (or more) circuits.
MHz	Mega Hertz, 10^6 cycles per second.
MIBUS	Mullard Instruction Bus; serial bus consisting of the information signal DATA and the accompanying clock signal DLIM. The MIBUS signals are delivered by the control system of the TV.
MIX mode	operating mode of the TV in which the TV picture is combined with teletext display. MIX mode can be switched on and off by means of a key on the remote control transmitter.
Multipage Acquisition	Search for several teletext pages simultaneously.
Next page	Control command for the CCT decoder that can be given with an additional key on the transmitter of the remote control (e.g. RC5373). With this command a searched teletext page that has been stored in the page memory, can be displayed on the screen.

NIL — Non Interlace; control signal to the time base of the TV to switch off interlacing in case of display of teletext in the TXT mode.

OE — Output Enable; control signal of the CCT IC to the page memory to switch on the data output buffers of the page memory.

O/E — ODD/EVEN; control signal from the CCT IC indicating if an odd or an even frame is displayed on the screen. The signal is used for the formation of the NIL signal.

P — Stop; indication for the stop procedure in case of the IIC bus transmissions.

PL — Phase Lock; part of the SAND signal for phase locking of the F6 clock with the TV signal and for switching off of the Data Slicer in VIP2 in case of poor signal quality.

PLL — Phase Locked Loop; control loop on the basis of phase comparison.

er On Reset — Bringing a circuit or an IC in a defined initial state after the power supply voltage has been switched on.

Pull-down — Lowering the voltage level at a certain point in a circuit, for instance by connecting this point by means of a resistor to a point with a lower voltage level.

Pull-up — Raising the voltage level at a certain point in a circuit, for instance by connecting this point by means of a resistor to a point with a higher voltage level.

R — Read; indication for the direction of the data in case of IIC bus transfers.

RAM — Random Access Memory; memory that can be used for both writing away and reading back data. When the power supply of the memory is switched off, the stored data are lost.

RC-5 — Remote Control system no 5; coding system for remote control commands. Consists of a serial data signal.

RGB — Red, Green, Blue; television colour signals.

ROM — Read Only Memory; memory that can only be used to read back data. The memory contents has been applied once and is preserved even when the power supply of the memory is switched off.

ROW — text row, consisting of maximum 40 teletext characters.

RUN — Active state of the microcomputer. In the RUN state the microcomputer executes its programme.

S — Start; indication for the start procedure in case of IIC transfers.

SAND — Sandcastle; three-level, line frequent synchronisation signal from the CCT IC. The SAND signal is used for phase locking of the F6 clock on the TV signal and, furthermore, to switch off the Data Slicer in VIP2 in case a poor quality of the received teletext data has been established.
As to waveform the SAND signal corresponds with the sandcastle signal from the TV technique but should not be confused with it as to function.

SCL — Serial Clock; serial clock signal of the IIC bus.

SCS — Scan Composite Sync; composite sync signal that can be presented to VIP2 and CCT IC from an external signal source. In teletext applications of VIP2 and CCT IC this signal is not used.

SDA — Serial Data; serial data signal of the IIC bus.

Single page Decoder — Teletext decoder that can search for one page at a time.

Software — Programmes of the microcomputer.

Status — Mode or position.

Status row — Additional text row with data on the control mode of the teletext decoder. The status row is displayed below or above the main text.

STTV — Sync To TV; composite sync signal from VIP2 for synchronization of the TV in case of display of teletext.

SVCT — Simple Viewdata Compatible Teletext decoder.

Sync — Synchronization.

System 4 — Colour television receiver system based on TV chassis KT4 and K40.

TAC — Teletext Data Acquisition and Control; IC with typenumber SAA 5041 which, among other things, sees to acquisition and control of the teletext data in the TIC TAC TROM teletext decoder.

TCS — Text Composite Sync; composite sync signal from the CCT IC for synchronization of the TV in case of display of teletext.

TIC — Timing Chain; IC with typenumber SAA 5020 which, among other things, sees to the timing in the TIC TAC TROM teletext decoder.

TIC TAC TROM decoder — Teletext decoder based on the VIP1, the TIC, the TAC and the TROM IC. This single page decoder is generally applied in TV receivers with KT3, K30, K35, KT4 and K40 chassis.

TROM — Teletext Read Only Memory; character generator IC in the TIC TAC TROM teletext decoder with type number SAA 5050/51/52/53.

TTC	Teletext Clock; clock signal from the VIP2 IC. The TTC signal which has a frequency of 6,9375 MHz, is used for the timing of the teletext data signal TTD.
TTD	Teletext Data; serial data signal from the VIP2 IC which contains the teletext data that the VIP2 IC has retrieved from the TV signal.
TV	Television.
TXT	Teletext.
TXT mode	Mode of the TV receiver in which teletext data are displayed on the screen.
VIP1	Video Input Processor; IC with type-number SAA 5030 which is in the TIC TAC TROM decoder among other things used to retrieve the teletext signal from the video signal.
VIP2	Video Input Processor Version 2; IC with type number SAA 5230. VIP2 is an improved version of VIP1. VIP2 is in the CCT decoder among other things used to retrieve the teletext signal from the video signal.
VCO	Voltage Controlled Oscillator; oscillator whose output frequency is determined by the extent of a control voltage.
VCR	Video Cassette Recorder; input on the CCT IC that is used for switching over a time constant in the CCT IC when the teletext signal of a video recorder has to be processed.
VCS	Video Composite Sync; composite sync signal which the VIP2 retrieves from the CVBS signal. The VCS signal is used for field synchronization of the CCT IC and for quality guarding of the teletext data signal.
W	Write; indication for the direction of the data in case of IIC bus transfers.
WE	Write Enable; control signal from the CCT IC to the page memory to switch on the data input buffers of the page memory.
Y	Luminance signal for the TV picture.